

**Preliminary**

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晶采光電科技股份有限公司

AMPIRE CO., LTD

# **SPECIFICATIONS FOR LCD MODULE**

<b>CUSTOMER</b>	
<b>CUSTOMER PART NO.</b>	
<b>AMPIRE PART NO.</b>	<b>AM-240320LGTNQW-00H</b>
<b>APPROVED BY</b>	
<b>DATE</b>	

☒ Approved For Specifications

☐ Approved For Specifications & Sample

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Revision Date	Page	Contents	Editor
2011/08/19	-	New Release	Rober

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# 1 Features

LCD 2.4 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments.

- (1) Construction: 2.4" a-Si color TFT-LCD, White LED Backlight and FPCB.
- (2) Main LCD : 2.1 Amorphous-TFT 2.4 inch display, transmissive, Normally white type, 12 o'clock.
  - 2.2 240(RGB)X320 dots Matrix, 1/320 Duty.
  - 2.3 Narrow-contact ledge technique.
  - 2.4 Main LCD Driver IC: HX8347-D
  - 2.5 262K: Red-6bit, Green-6bit, Blue-6bit (18-bit interface)
- (3) Low cross talk by frame rate modulation
- (4) Direct data display with display RAM
- (5) Partial display function: You can save power by limiting the display space.
- (6) Interface: MPU and RGB Interface. (Select by H/W Jumper). **Default : SPI**

Interface mode	JP0(IM0)		JP1(IM1)		JP2(IM2)		JP3(IM3)		Remark
	R1(H)	R2(L)	R3(H)	R4(L)	R5(H)	R6(L)	R7(H)	R8(L)	
80-16BIT Type I	NC	0R	NC	0R	NC	0R	NC	0R	
80-8BIT Type I	0R	NC	NC	0R	NC	0R	NC	0R	
80-16BIT Type II	NC	0R	0R	NC	NC	0R	NC	0R	
80-8BIT Type II	0R	NC	0R	NC	NC	0R	NC	0R	
3-wire SPI	NC	0R	NC	0R	0R	NC	NC	0R	Default
4-wire SPI	-	-	0R	NC	0R	NC	NC	0R	
80-18BIT Type I	NC	0R	NC	0R	NC	0R	0R	NC	
80-9BIT Type I	0R	NC	NC	0R	NC	0R	0R	NC	
80-18BIT Type II	NC	0R	0R	NC	NC	0R	0R	NC	
80-9BIT Type II	0R	NC	0R	NC	NC	0R	0R	NC	

- (7) Abundant command functions:

Area scroll function

Display direction switching function

Power saving function

Electric volume control function: you are able to program the temperature compensation function.

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## 2 Mechanical specifications

### Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 43.6 (W) x 85.5 (H) x2.8(T)	mm
Main LCD	Pixel size	0.153 (W) x 0.153 (H)	mm
	Active area	36.72 (W) x 48.96 (H)	mm
	Number of Pixels	240(H)x320(V) pixels	mm
Weight		T.B.D.	g

\*1. This specification is about External shape on shipment from AMPIRE.

## 3 Absolute max. ratings and environment

### 3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+4	V	Logic I/O power supply
Power voltage	VCI–GND	-0.3	+4	V	Driver power supply
Power voltage	LED A – LED K	-0.5	+15	V	

### 3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +80 °C Min. -30 °C	Note 1: Non-condensing
Operating temperature	Max. +70 °C Min. -20 °C	Note 1: Non-condensing

Note 1 : Ta ≤ +40 °C . . . . Max.85%RH

Ta > +40 °C . . . . The max. humidity should not exceed the humidity with 40 °C 85%RH.

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**4 Electrical specifications****4-1 Electrical characteristics of LCM**

( $V_{DD}=3.0V$ ,  $T_a=25^{\circ}C$ )

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage(Power)	$V_{DD}$		2.3	2.8	3.3	V
IC power voltage(Logic)	$V_{CI}$		2.3	2.8	3.3	V
High-level input voltage	$V_{IHC}$		0.8		$V_{DD}$	V
Low-level input voltage	$V_{ILC}$		-0.3		$0.2V_{DD}$	V
Consumption current of VDD	$I_{DD}$	LED OFF	-	8	15	mA
Consumption current of LED	$I_{LED\_ON}$	$V_{LED}=12.8V$	-	20	-	mA

※ 1. 1/320 duty.

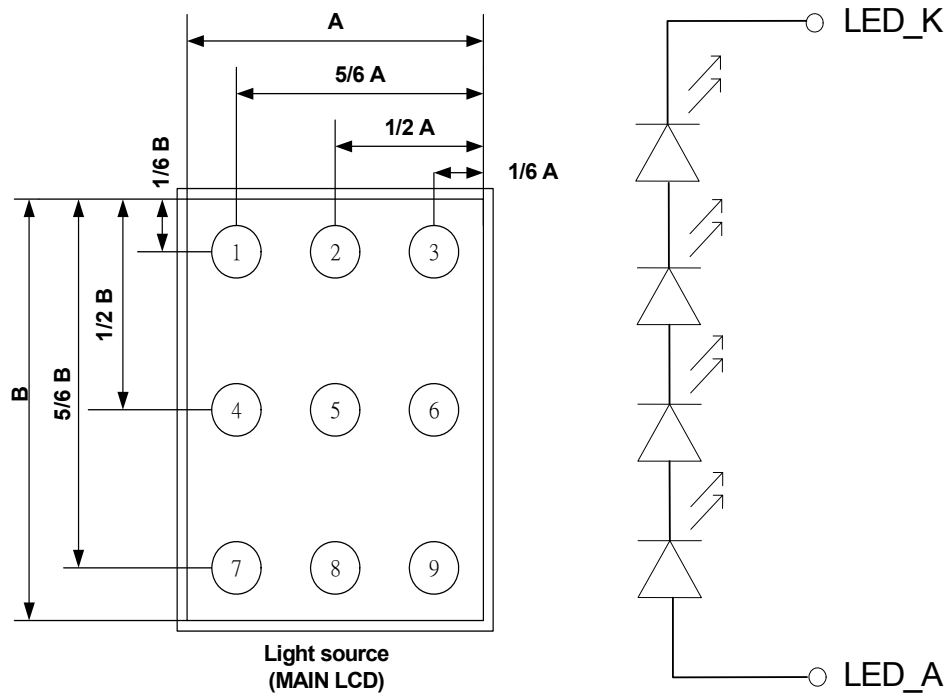
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### 4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	$V_f$	$I_f = 20\text{mA}$	12.3	12.8	13.8	V
Reverse voltage	$V_r$		-	-	12	V
Forward current	$I_f$	4-chip serial	-	18	20	mA
Power Consumption	$P_{BL}$	$I_f = 20\text{mA}$	-	256	276	mW
Uniformity (with L/G)	-	$I_f = 20\text{mA}$	80%*1	-	-	
Bare LED Luminous intensity	$V_f$ $I_f$	13.2V 20mA	3700	-	-	cd/m <sup>2</sup>
Luminous color	White					
Chip connection	4 chip serial connection					

Bare LED measure position:



\*1 Uniformity (LT):  $\frac{\text{Min}(P1 \sim P9)}{\text{Max}(P1 \sim P9)} \times 100 \geq 80\%$

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# 5 Main LCD

## 5-1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

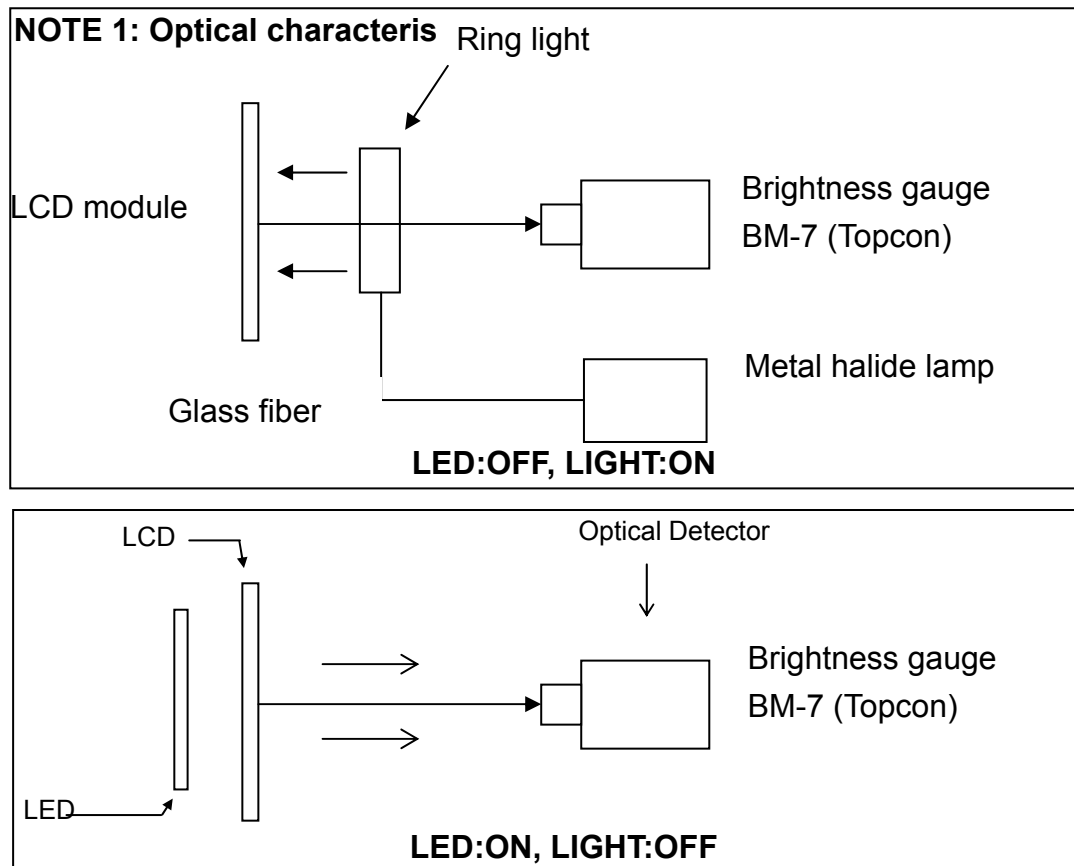
Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25 °C	--	15	25	ms	$\theta=0^{\circ}$ , $\varphi=0^{\circ}$ (Note 2)
	Tf	25 °C	--	20	30		
Contrast ratio	CR	25 °C	-	200	-	-	$\theta=0^{\circ}$ , $\varphi=0^{\circ}$ LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25 °C	-	4.7	-	%	
Visual angle range front and rear	$\theta$	25 °C	(θf) 35(20) (θb) 65(45)			De-gree	$\varphi=0^{\circ}$ , CR $\geq$ 10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	$\theta$	25 °C	(θl) 70(45) (θr) 70(45)			De-gree	$\varphi=90^{\circ}$ , CR $\geq$ 10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			170	220	--	Cd/m <sup>2</sup>	I <sub>F</sub> =20mA, Full White pattern

## 5-2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

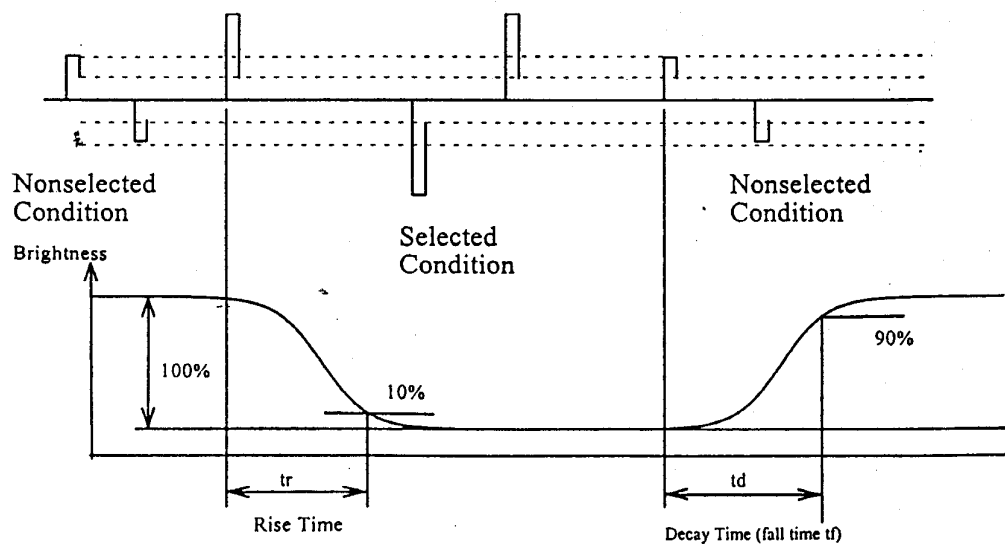
Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	0.5789	0.6289	0.6789	$\theta=0^{\circ}$ , $\varphi=0^{\circ}$
	Y	0.2946	0.3446	0.3946	
Green	X	0.2968	0.3468	0.3968	$\theta=0^{\circ}$ , $\varphi=0^{\circ}$
	Y	0.5293	0.5793	0.6293	
Blue	X	0.1095	0.1595	0.2095	$\theta=0^{\circ}$ , $\varphi=0^{\circ}$
	Y	0.0975	0.1475	0.1975	
White	X	0.261	0.311	0.361	$\theta=0^{\circ}$ , $\varphi=0^{\circ}$
	Y	0.2971	0.3471	0.3971	

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## NOTE 2: Response tome definition

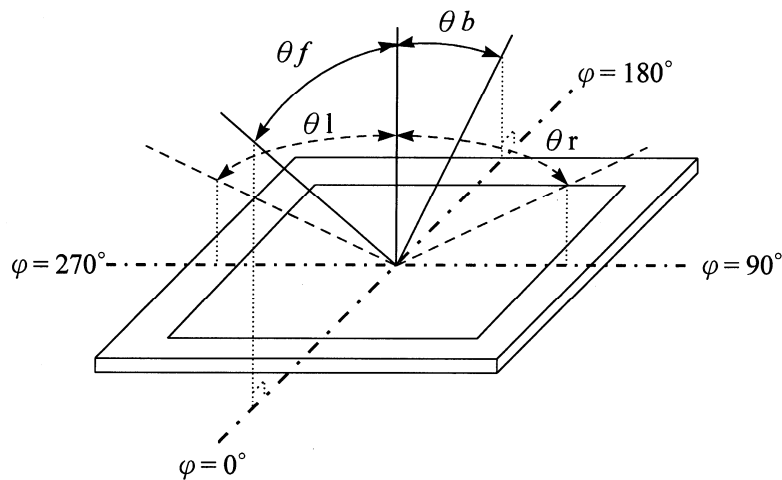




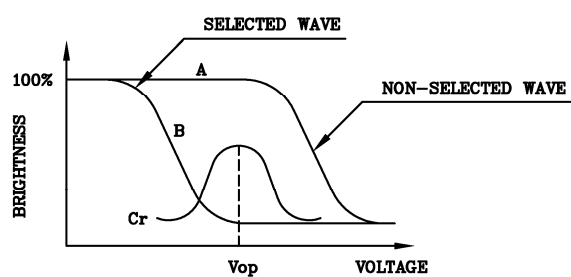
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### NOTE 3: $\varphi$ 、 $\theta$ definition

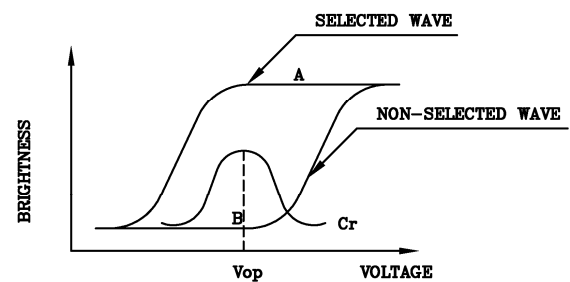


### NOTE 4: Contrast definition



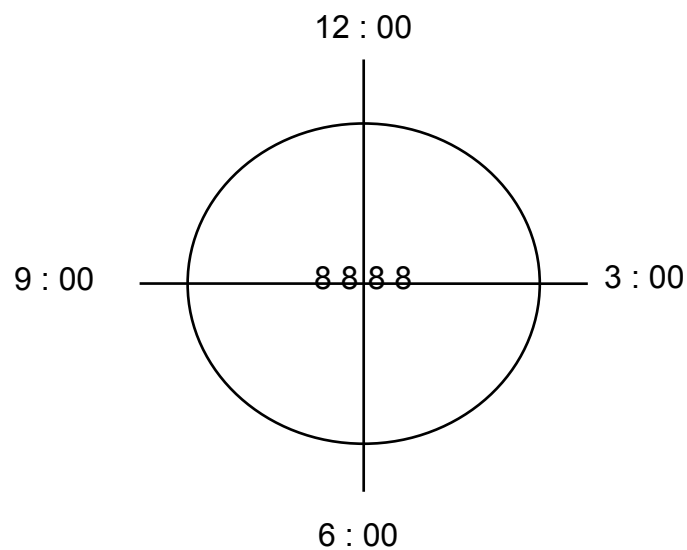
(positive type)

Contrast Ratio :  $Cr=A/B$



(negative type)

### NOTE 5: Visual angle direction priority



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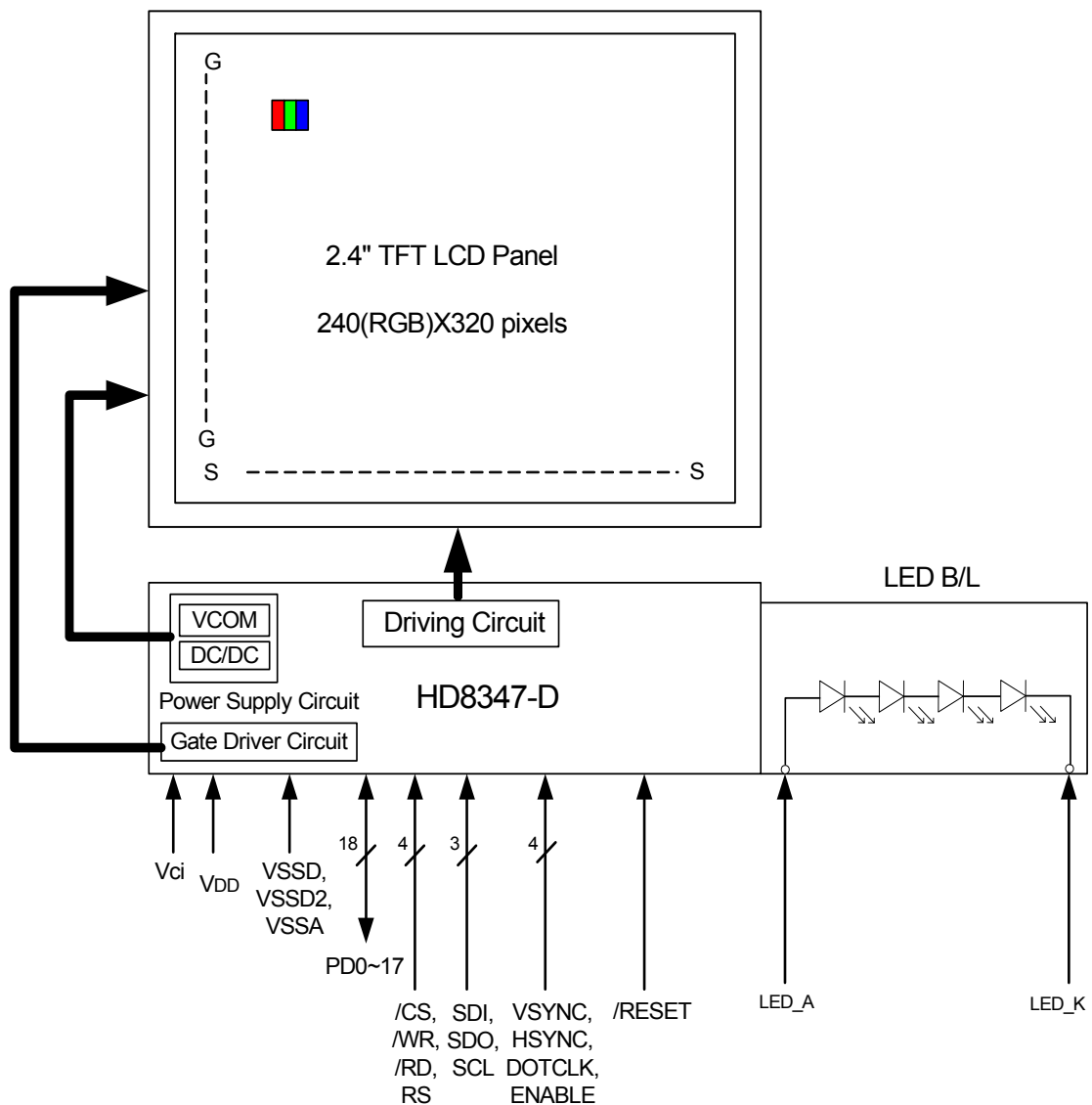
## 6 Block Diagram

### Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.

Display composition: 240 x RGB x 320 dots

LCD Driver : HX8347-D



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## 7 Interface specifications

Pin No.	Terminal	Functions																														
1	ENABLE	A data ENABLE signal in RGB I/F mode.																														
2	DOTCLK	Dot clock signal in RGB I/F mode.																														
3	HSYNC	Frame synchronizing signal in RGB I/F mode.																														
4	VSYNC	Frame synchronizing signal in RGB I/F mode.																														
5	/CS	Chip select signal.																														
6	WR/SCL	Write enable signal/Serial bus interface clock input pin.																														
7	SDI	Serial bus interface data input pin.																														
8	RS	Command/display Data Selection.																														
9	NC	NC																														
10	/RD	Read enable signal.																														
11	/RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.																														
12	PD0	<table><tr><th>Mode</th><th>IM[3:0]</th><th>PD Pin in use</th></tr><tr><td>MCU 18-bit Type I</td><td>1000</td><td>PD [17:0]</td></tr><tr><td>MCU 16-bit Type I</td><td>0000</td><td>PD [15:10]</td></tr><tr><td>MCU 9-bit Type I</td><td>1001</td><td>PD [8:0]</td></tr><tr><td>MCU 8-bit Type I</td><td>0001</td><td>PD [7:0]</td></tr><tr><td>MCU 18-bit Type II</td><td>1010</td><td>PD [17:0]</td></tr><tr><td>MCU 16-bit Type II</td><td>0010</td><td>PD [17:10], DB[8:1]</td></tr><tr><td>MCU 9-bit Type II</td><td>1011</td><td>PD [17:9]</td></tr><tr><td>MCU 8-bit Type II</td><td>0011</td><td>PD [17:10]</td></tr><tr><td>Serial Mode/Digital RGB Interface Mode</td><td>0101</td><td>SDI, SDO, SCL R[5:0]=PD[17:12] G[5:0]=PD[11:6] B[5:0]=PD[5:0]</td></tr></table>	Mode	IM[3:0]	PD Pin in use	MCU 18-bit Type I	1000	PD [17:0]	MCU 16-bit Type I	0000	PD [15:10]	MCU 9-bit Type I	1001	PD [8:0]	MCU 8-bit Type I	0001	PD [7:0]	MCU 18-bit Type II	1010	PD [17:0]	MCU 16-bit Type II	0010	PD [17:10], DB[8:1]	MCU 9-bit Type II	1011	PD [17:9]	MCU 8-bit Type II	0011	PD [17:10]	Serial Mode/Digital RGB Interface Mode	0101	SDI, SDO, SCL R[5:0]=PD[17:12] G[5:0]=PD[11:6] B[5:0]=PD[5:0]
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MCU 16-bit Type II	0010		PD [17:10], DB[8:1]																													
MCU 9-bit Type II	1011		PD [17:9]																													
MCU 8-bit Type II	0011		PD [17:10]																													
Serial Mode/Digital RGB Interface Mode	0101		SDI, SDO, SCL R[5:0]=PD[17:12] G[5:0]=PD[11:6] B[5:0]=PD[5:0]																													
13	PD1																															
14	PD2																															
15	PD3																															
16	PD4																															
17	PD5																															
18	PD6																															
19	PD7																															
20	PD8																															
21	PD9																															
22	PD10																															
23	PD11																															
24	PD12																															
25	PD13																															
26	PD14																															
27	PD15																															
28	PD16																															
29	PD17																															

(To be continued)

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30	VDD	Power supply for the internal logic circuit. (VDD=1.65~3.3V)
31	VCI	Power supply for Step-up circuit. (VCI=2.3~3.3V)
32	VCI	
33	NC	NC
34	NC	
35	NC	
36	NC	
37	NC	
38	NC	
39	NC	
40	GND	GND-terminal
41	NC	NC
42	NC	
43	NC	
44	NC	
45	GND	GND-terminal
46	SDO	Serial bus interface data output pin.
47	NC	NC
48	NC	
49	NC	
50	GND	GND-terminal
51	GND	

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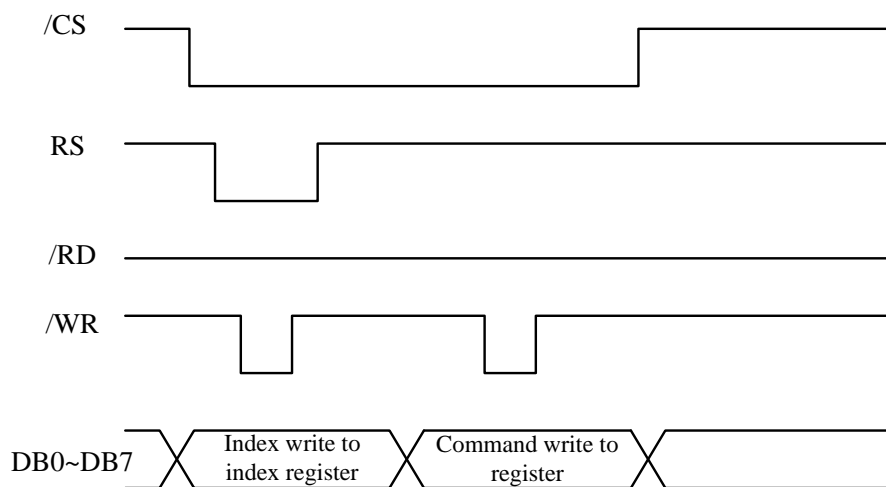
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### 7-1 Parallel bus system interface

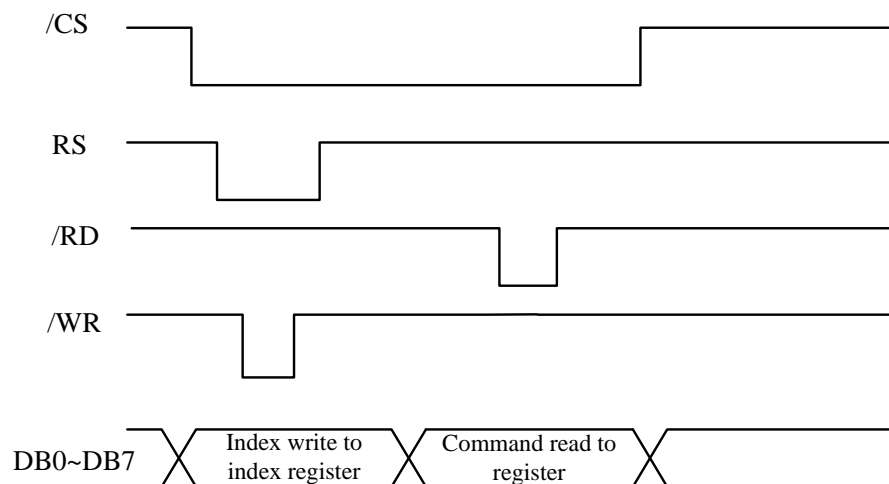
The input / output data from data pins (DB17-0) and signal operation of the I80 series parallel bus interface are listed as below.

Operations	WR/SCL	/RD	RS
Writes Indexes into IR	0	1	0
Reads internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Write to register



Read to register

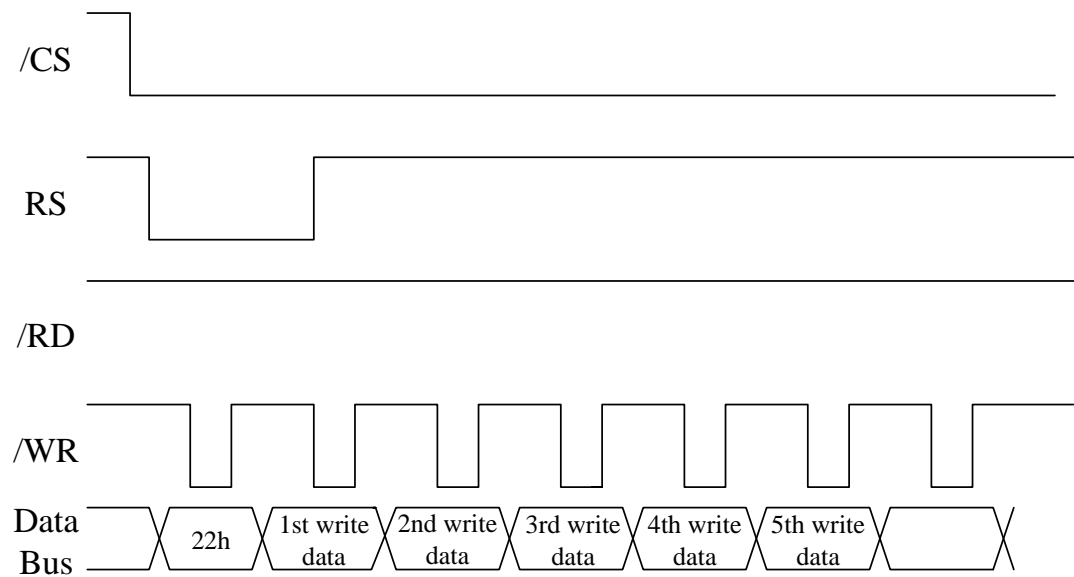


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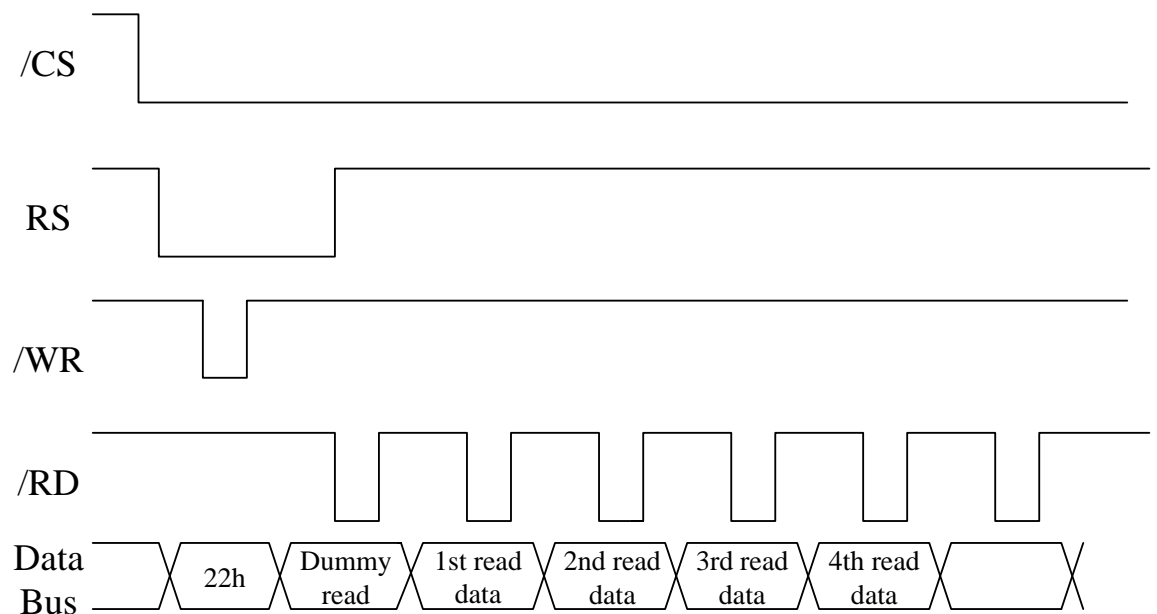
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### Write to the graphic RAM



### Read to the graphic RAM



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## 7-2 MCU data color coding

MCU Data Color Coding for RAM data **Write**

- Parallel 8-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
17H	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	Color
05h	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	4K-Color (2-pixels/ 3-bytes)
06h	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	65K-Color (1-pixel/ 2-bytes)
	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.3 8-bit parallel interface type I GRAM write table

- Parallel 16-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
17H	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
03h											R3	R2	R1	R0	G3	G2	G1	G0	Color
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	4K-Color
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	65K-Color
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
07h	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	262K-Color (16+2)
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B1	B0	

Table 5.4 16-bit parallel interface type I GRAM write table

- Parallel 9-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
17H	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	Color
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	262K-Color (1-pixels/ 2bytes)

Table 5.5 9-bit parallel interface type I GRAM write table

- Parallel 18-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
17H	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	Color
																			262K-Color

Table 5.6 18-bit parallel interface type I GRAM write table

- Parallel 8-Bit Bus Interface type II (IM3,IM2,IM1,IM0="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
17H	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	22H
03h	R3	R2	R1	R0	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	Color
05h	B3	B2	B1	B0	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	4K-Color (2-pixels/ 3-bytes)
	G3	G2	G1	G0	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixel/ 2-bytes)
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5.7 8-bit parallel interface type II GRAM write table

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### - Parallel 16-Bit Bus Interface typeII (IM3,IM2,IM1,IM0="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	22H
03h	X	x	x	x	R3	R2	R1	R0	x	G3	G2	G1	G0	B3	B2	B1	B0	x	Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	4K-Color
06h	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	65K-Color
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	262K-Color (2-pixels/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	
07h	R5	R4	R3	R2	R1	R0	G5	G4	x	G3	G2	G1	G0	B5	B4	B3	B2	x	262K-Color (16+2)
	B1	B0	x	x	x	x	x	x	x	x	x	x	x			x	x	x	

Table 5.8 16-bit parallel interface type II GRAM write set table

### - Parallel 9-Bit Bus Interface typeII (IM3,IM2,IM1,IM0="1011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
17H	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	22H
06h	D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5.9 9-bit parallel interface set type II GRAM write table

### - Parallel 18-Bit Bus Interface typeII (IM3,IM2,IM1,IM0="1010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
17H	X	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	22H
06h	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.10 18-bit parallel interface type II GRAM write set table



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### 7-3 80-system 18-bit interface

The I80-system 18-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “1000”. And the I80-system 18-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, and IM0” pins to “1010”. Figure 5.3 is the example of interface with I80 microcomputer system interface.

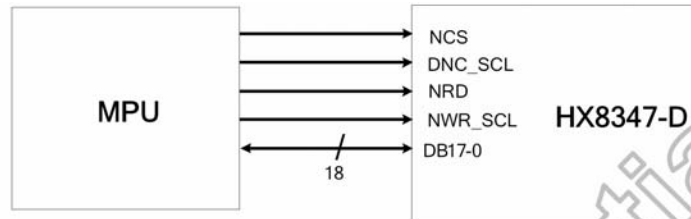


Figure 5.3 Example of I80- system 18-bit parallel bus interface

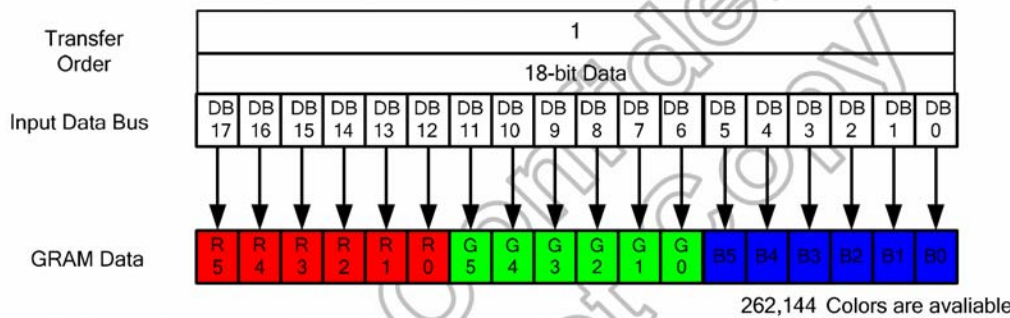


Figure 5.4 Input data bus and GRAM data mapping in 18-bit bus system interface with 18-bit-data Input (“IM3, IM2, IM1, IM”=“1010” or “1000”)

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### 7-4 80-system 16-bit interface

The I80-system 16-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “0000”.

And I80-system 16-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “0010”. Figure 5.5 is the example of type I interface with I80 microcomputer system interface. And Figure 5.6 is the example of type II interface with I80 microcomputer system interface.

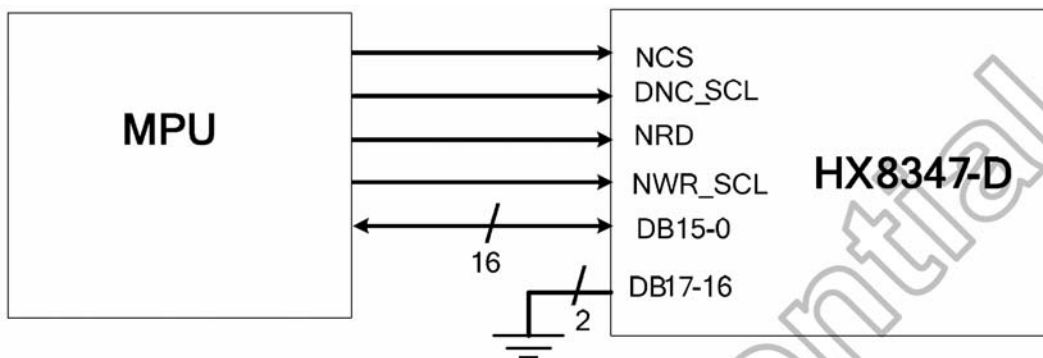


Figure 5.5 Example of I80 system 16-bit parallel bus interface type I

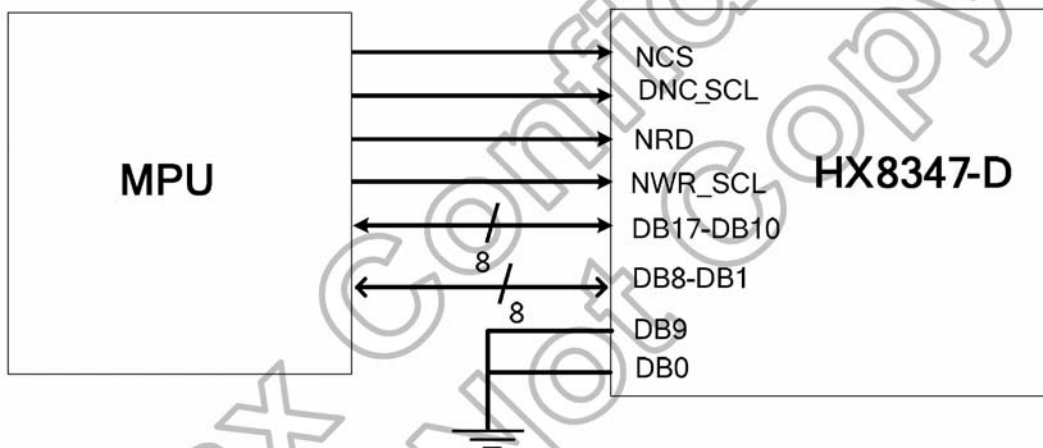


Figure 5.6 Example of I80 system 16-bit parallel bus interface type II

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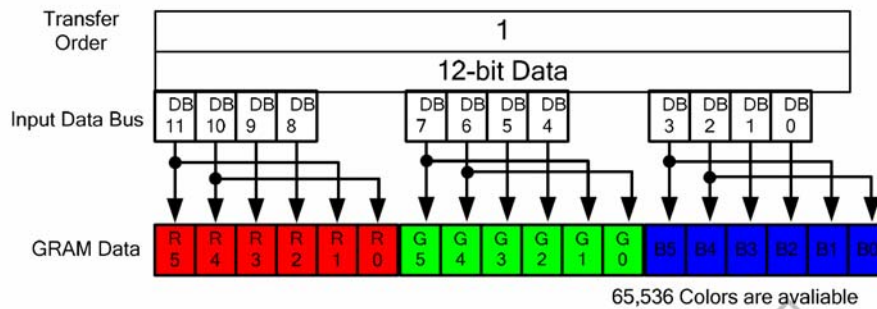


Figure 5.7 Input data bus and GRAM data mapping in 16-bit bus system interface with 12-bit-data input (**R17H=03h** and "IM3, IM2, IM1, IM0"="0000")

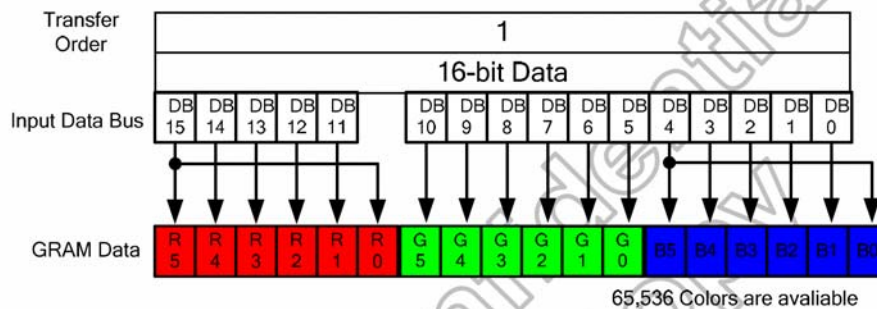


Figure 5.8 Input data bus and GRAM data mapping in 16-bit bus system interface with 16-bit-data input (**R17H=05h** and "IM3, IM2, IM1, IM0"="0000")

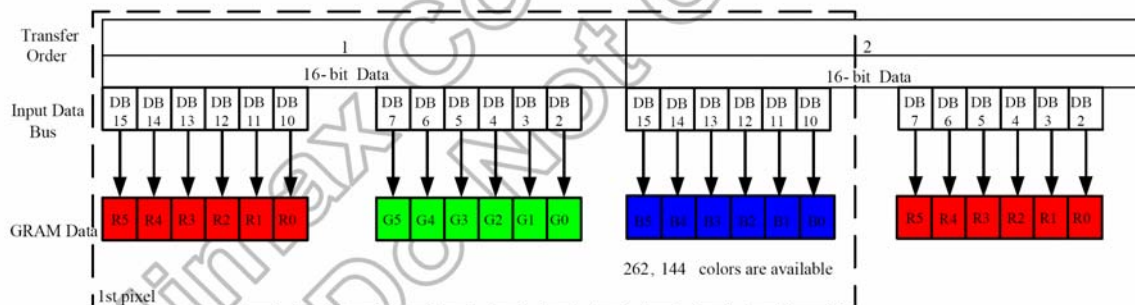


Figure 5.9 Input data bus and GRAM data mapping in 16-bit bus system interface with 18 bit-data input (**R17H=06h** and "IM3, IM2, IM1, IM0"="0000")

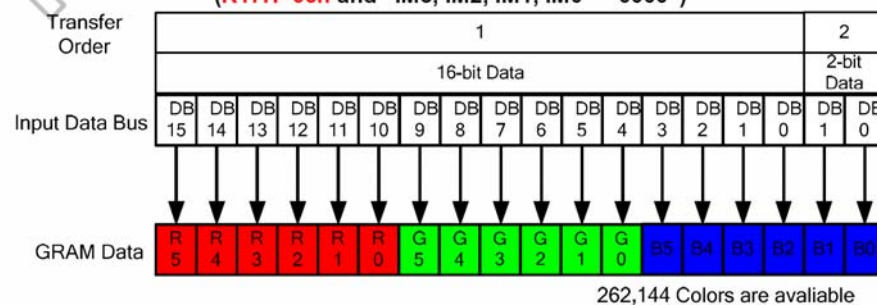


Figure 5.10 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (**R17H=07h** and "IM3, IM2, IM1, IM0"="0000")

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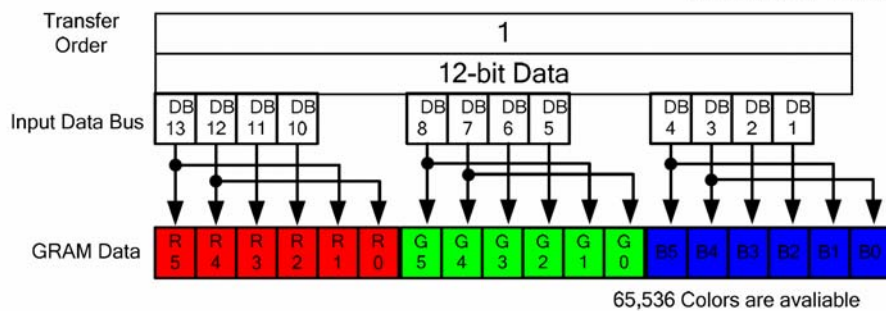


Figure 5.11 Input data bus and GRAM data mapping in 16-bit bus system interface with 12-bit-data input (R17H=03h and "IM3, IM2, IM1, IM0"="0010")

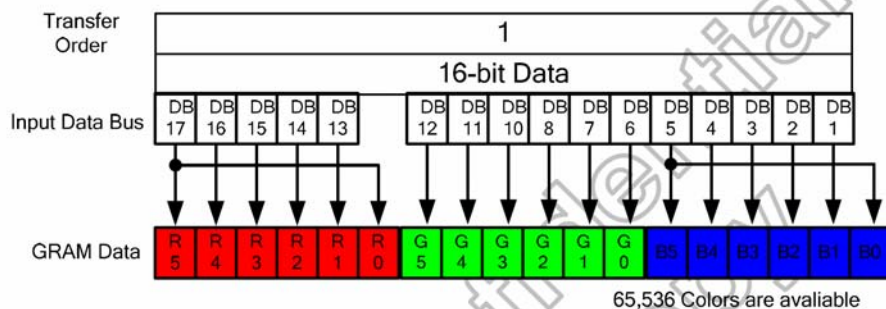


Figure 5.12 Input data bus and GRAM data mapping in 16-bit bus system interface with 16-bit-data input (R17H=05h and "IM3, IM2, IM1, IM0"="0010")

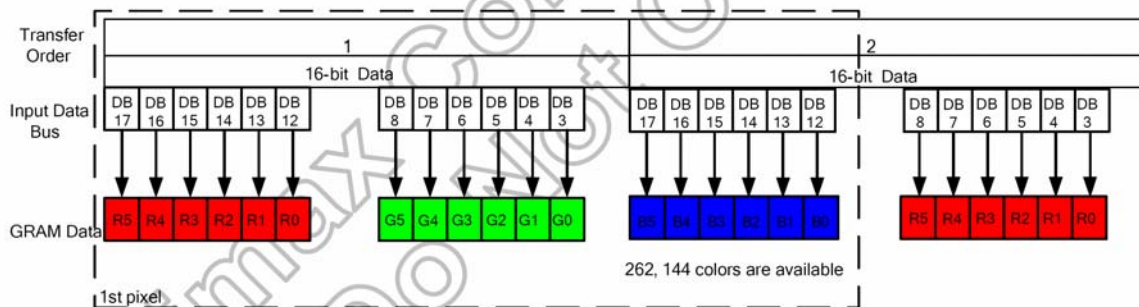


Figure 5.13 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(12+6) bit-data input (R17H=06h and "IM3, IM2, IM1, IM0"="0010")

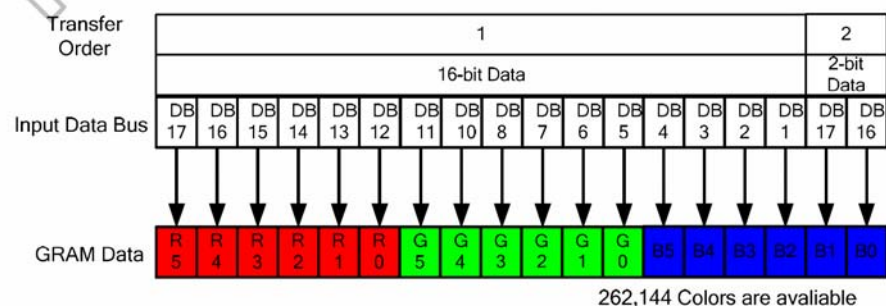


Figure 5.14 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (R17H=07h and "IM3, IM2, IM1, IM0"="0010")

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### 7-5 9-bit parallel bus system interface

The I80-system 9-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “1001”. And I80-system 9-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “1011”. Figure 5.15 is the example of type I interface with I80 microcomputer system interface. And Figure 5.16 is the example of type II interface with I80 microcomputer system interface.

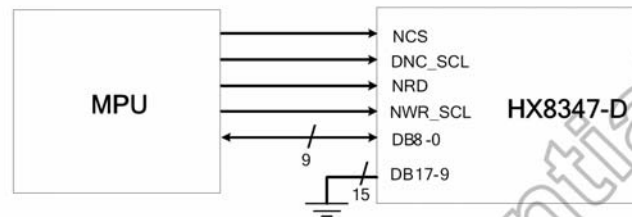


Figure 5.15 Example of I80 system 9-bit parallel bus interface type I

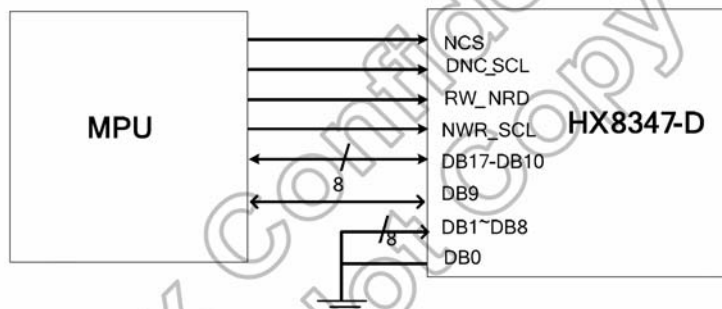


Figure 5.16 Example of I80 system 9-bit parallel bus interface type II

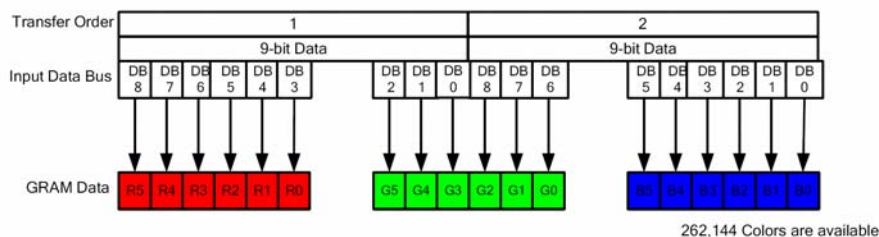


Figure 5.17 Input data bus and GRAM data mapping in 9-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=“1001”)

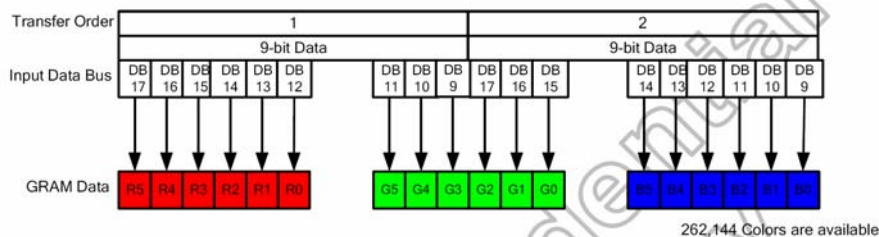


Figure 5.18 Input data bus and GRAM data mapping in 9-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=“1011”)



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### 7-6 8-bit Parallel Bus System Interface

The I80-system 8-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “0001”. And I80-system 8-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “0011”. Figure 5.19 is the example of type I interface with I80 microcomputer system interface. And Figure 5.20 is the example of type II interface with I80 microcomputer system interface.

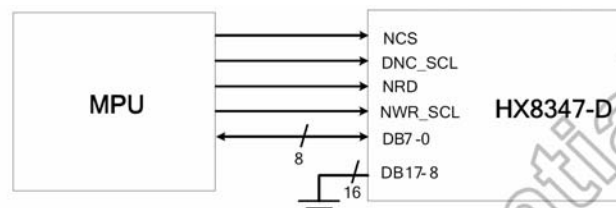


Figure 5.19 Example of I80 system 8-bit parallel bus interface type I

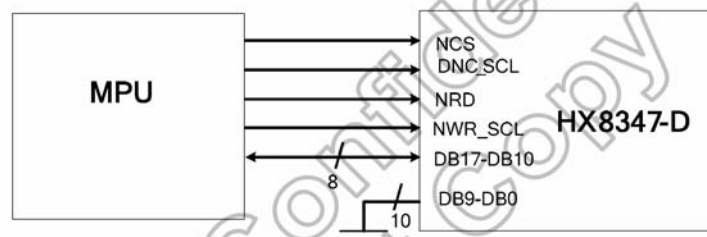


Figure 5.20 Example of I80 system 8-bit parallel bus interface type II

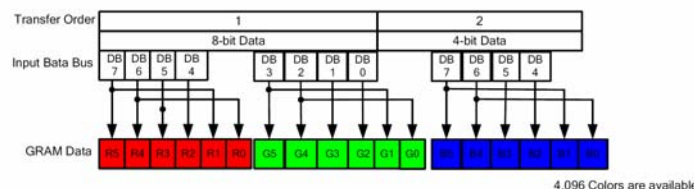


Figure 5.21 Input data bus and GRAM data mapping in 8-bit bus system interface with 12-bit-data input (R17H=03h and “IM3, IM2, IM1, IM0”=“0001”)

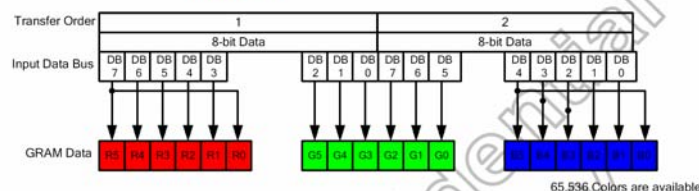


Figure 5.22 Input data bus and GRAM data mapping in 8-bit bus system interface with 16-bit-data input (R17H=05h and “IM3, IM2, IM1, IM0”=“0001”)

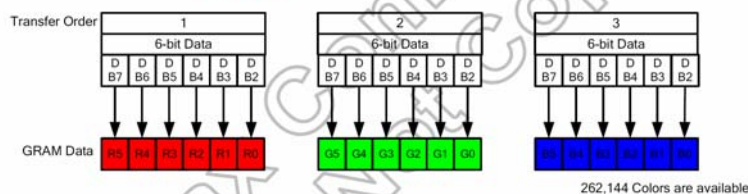


Figure 5.23 Input data bus and GRAM data mapping in 8-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=“0001”)

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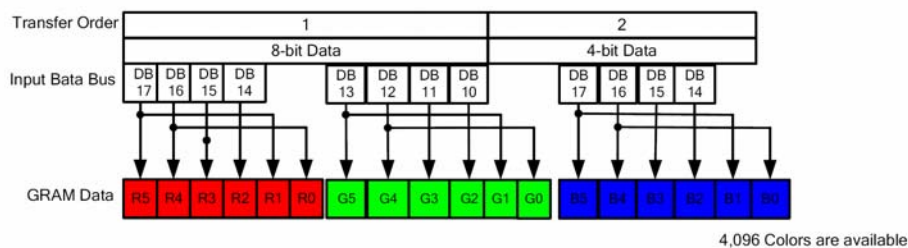


Figure 5.24 Input data bus and GRAM data mapping in 8-bit bus system interface with 12-bit-data input  
 (R17H=03h and "IM3, IM2, IM1, IM0"="0011")

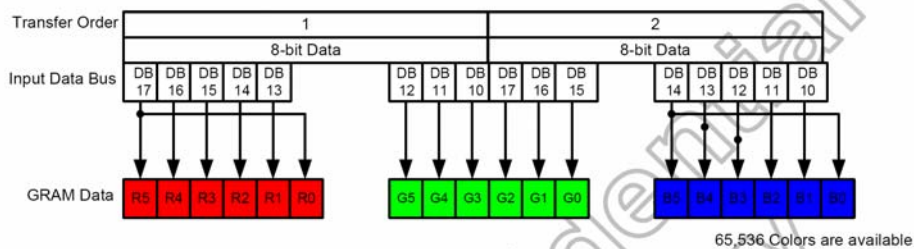


Figure 5.25 Input data bus and GRAM data mapping in 8-bit bus system interface with 16-bit-data input  
 (R17H=05h and "IM3, IM2, IM1, IM0"="0011")

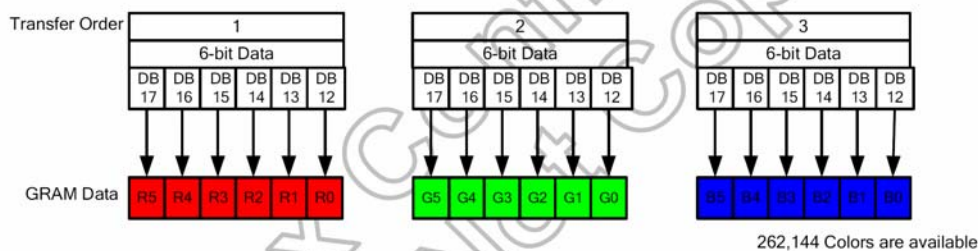


Figure 5.26 Input data bus and GRAM data mapping in 8-bit bus system interface with 18-bit-data input  
 (R17H=06h and "IM3, IM2, IM1, IM0"="0011")

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## 7-7 MCU Data Color Coding for RAM data Read

- Parallel 8-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.11 8-bit parallel interface type I GRAM read table

- Parallel 16-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.12 16-bit parallel interface type I GRAM read table

- Parallel 9-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.13 9-bit parallel interface type I GRAM read table

- Parallel 18-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	22H
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.14 18-bit parallel interface type I GRAM read table



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### - Parallel 8-Bit Bus Interface type II (IM3,IM2,IM1,IM0="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	22H
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x											262K-Color (1-pixel/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5.15 8-bit parallel interface type II GRAM read table

### - Parallel 16-Bit Bus Interface type II (IM3,IM2,IM1,IM0="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	22H
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixels/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 5.16 16-bit parallel interface type II GRAM read table

### - Parallel 9-Bit Bus Interface type II (IM3,IM2,IM1,IM0="1011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	22H
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5.17 9-bit parallel interface type II GRAM read table

### - Parallel 18-Bit Bus Interface type II (IM3,IM2,IM1,IM0="1010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	22H
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.18 18-bit parallel interface type II GRAM read table

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## 7-8 Serial bus system interface

The HX8347-D supports two kinds of serial bus interface in register-content mode by setting external pins “IM2, IM1” pins to “10” 3-wire serial interface and “IM2, IM1” pins to “11” 4-wire serial interface. The serial bus system interface mode is enabled through the chip select line (/CS), and it is accessed via a control consisting of the serial input data (SDA), and the serial transfer clock signal (WR/SCL).

### 7-8-1 3-wire serial interface

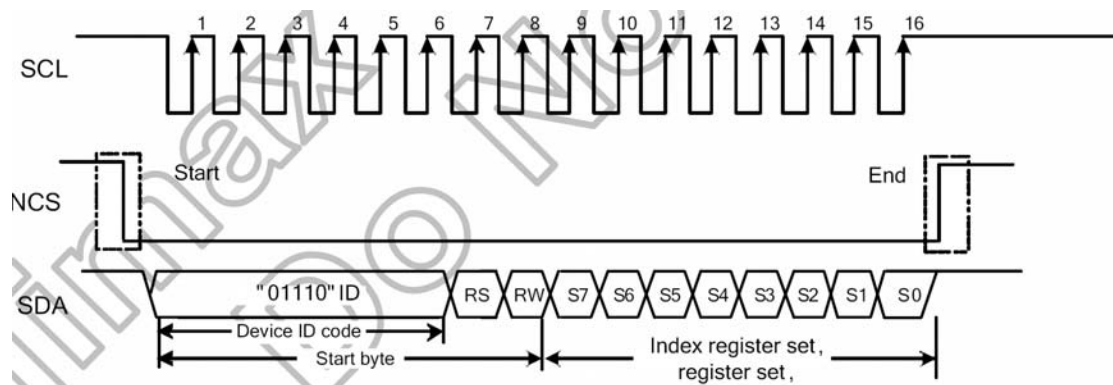
As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin IM0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status and it must be set to “1” when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

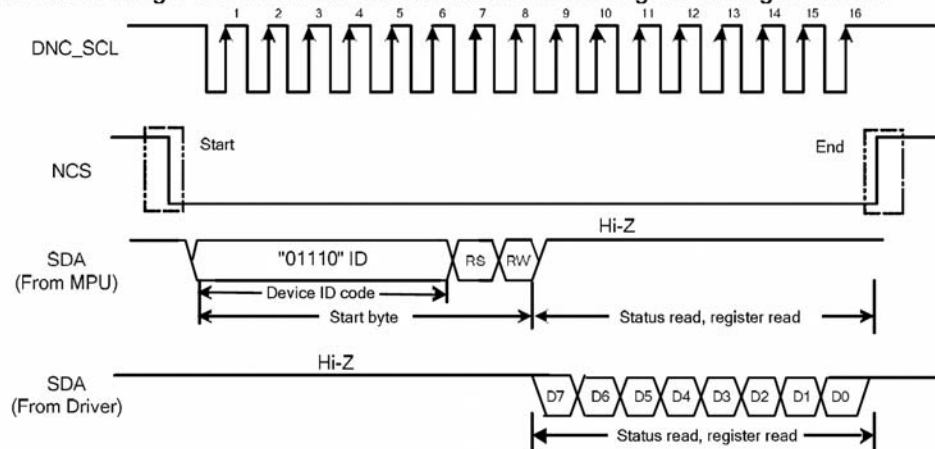
RS	R/W	Function
0	0	Set index register
1	0	Writes Instruction or GRAM data
1	1	Reads command (Not support GRAM read)

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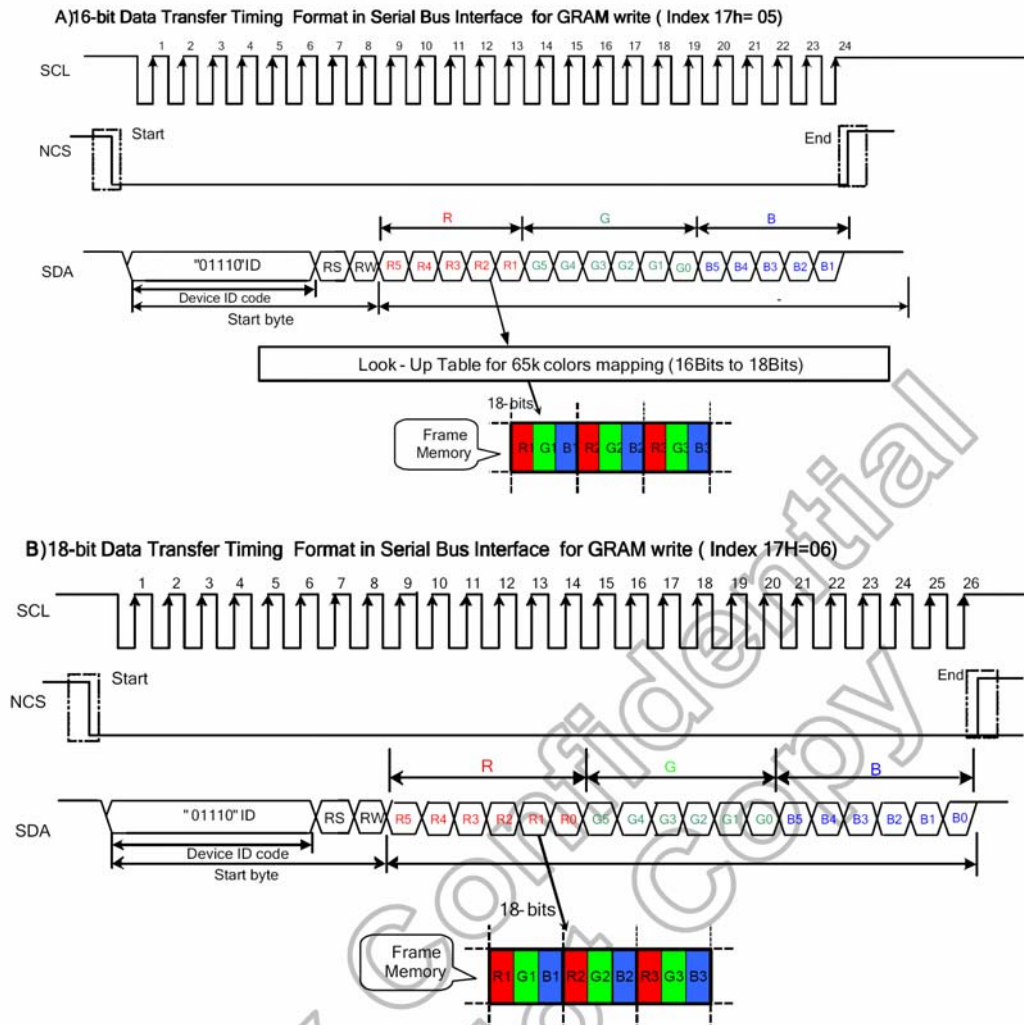


### B) Transfer Timing Format in Serial Bus Interface for Index Register or Register Read



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### 7-8-2 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by DNC pin. If DNC is low, the transmission byte is command byte. If DNC is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, NWR\_SCL clock pulse or SDA data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

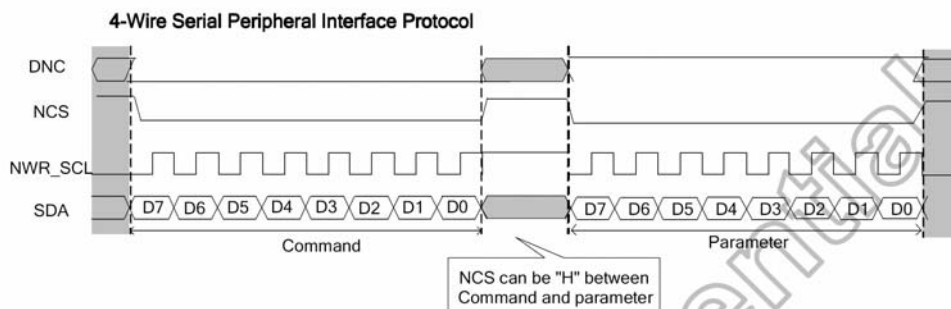


Figure 5.29 Index register write timing in 4-wire serial bus system interface

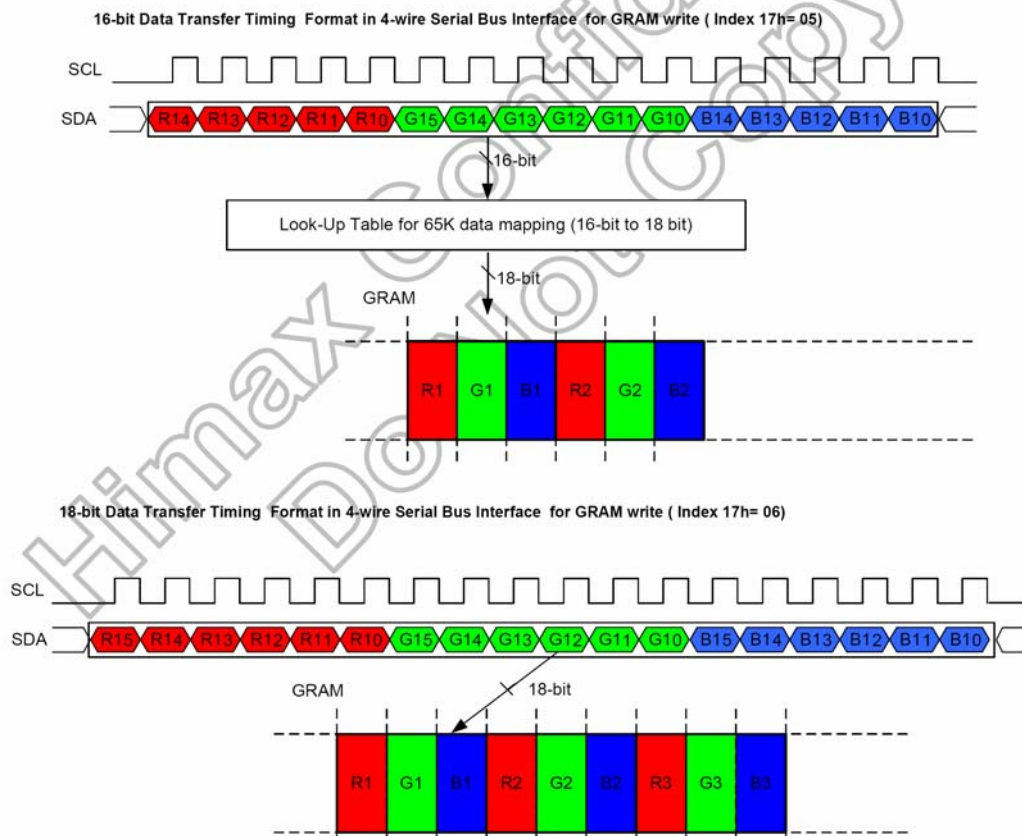


Figure 5.30 Data write timing in 4-wire serial bus system interface

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## 7-9 RGB Interface

The HX8347-D uses **RCM [1:0] = '10' or '11' hardware setting to select RGB interface**. After Power on Sequence, the RGB interface is activated. When RCM [1:0] = '10' use VSYNC, HSYNC, DE, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 1). When RCM [1:0] = '11' use VSYNC, HSYNC, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 2).

Pixel clock (DOTCLK) must be running all the time without stopping and it is used to entering VSYNC, HSYNC, DE and DB17-0 lines states when there is a rising edge of the DOTCLK.

In RGB interface mode 1, the valid display data is inputted in pixel unit via DB17-0 according to the high-level('H') of DE signal, and display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and pixel clock (DOTCLK). In RGB interface mode 2, the valid display data is inputted in pixel unit via DB17-0 according to the HBP setting of HSYNC signal, and the VBP setting of VSYNC. In these two RGB interface modes, the input display data is not written to GRAM and is displayed directly.

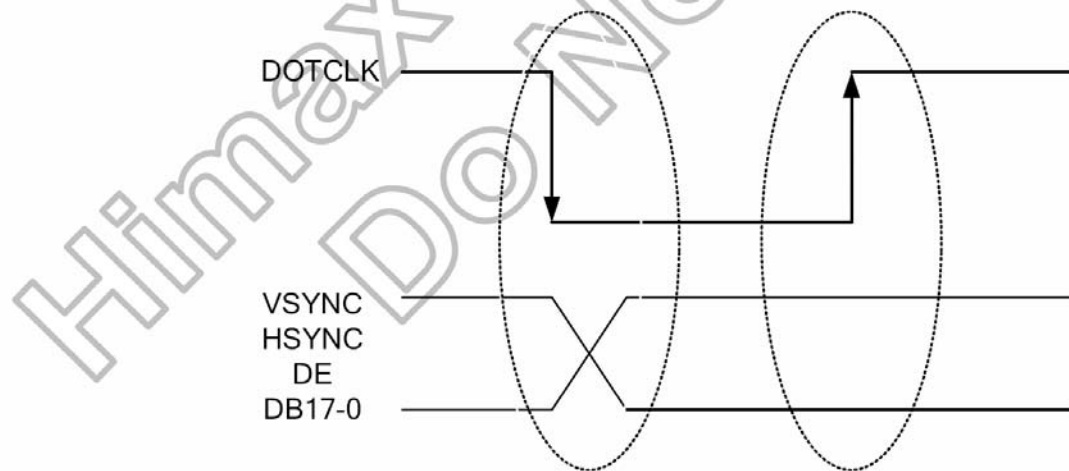
Vertical synchronization (VSYNC) signal is used to tell when there a new frame of the display is received, and this is negative ('-', '0', low) active. Horizontal synchronization signal (HSYNC) is used to tell when a new line of the frame is received, and this is negative ('-', '0', low) active. Data enable (DE) is used to tell when RGB information is received that should be transferred on the display, and this is positive ('+', '1', high) active. DB17-0 are used to tell what the information of the image is, that is transferred on the display when DE='H'.



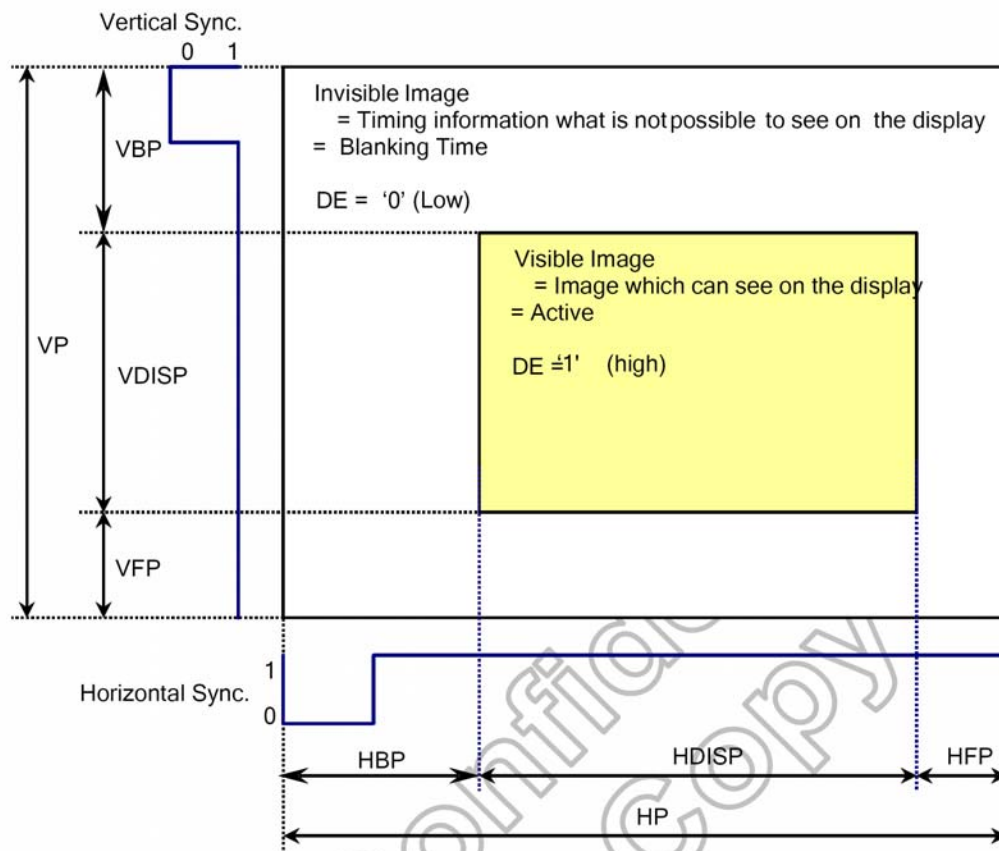
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The pixel clock cycle is described in the following figure.



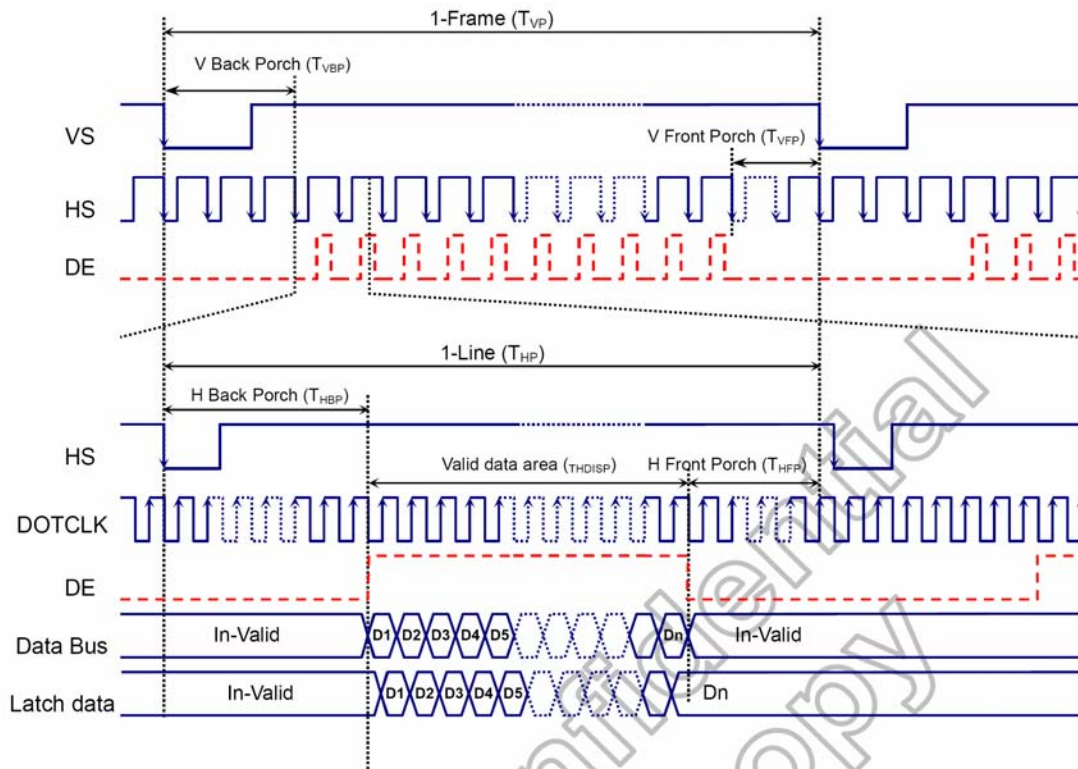
General timing diagram in RGB interface is as follow.



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The image information is correct on the display when the timings are in range on the interface. However, the image information will be incorrect on the display, when timings are out of the range on the RGB interface and the correct image information will be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range RGB interface timings.



**Note:** (1) RGB mode 2 doesn't need DE signal  
(2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of SETRGBIF (32H) command.

All 3 kinds of bus width can be available during RGB interface mode (selected by COLMOD (17H) command for 6-bit, 16-bit and 18-bit data width)

17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
50h	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bit data
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data
17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
E0h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bit data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

**Note:** (1) When 17H="E0h", 6-bit data width of 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.  
(2) Only 17H= "50h", "60h", "E0h" are valid on RGB I/F, others are invalid.



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### RGB interface mode

RGB I/F Mode	DOTCLK	DE	VS	HS	Video Data bus DB [B:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

There are 2 kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

**In RGB Mode 1** (RCM1, RCM0 = "10"), writing data to display is done by DOTCLK and Video Data Bus (DB [17:0]), when DE is high state. The external synchronization signals (DOTCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer DOTCLK, VS, HS and DE signals to driver.

**In RGB Mode 2** (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by R33h and R34h command. DE pin is not used.

### 7-10 Color order on RGB interface

The meaning of the pixel information, when 3 components/pixel (Red, Green and Blue) on RGB interface are used, is describing on the following table:

Pixel Color	R Component	G Component	B Component
Black	All bits are 0	All bits are 0	All bits are 0
Blue	All bits are 0	All bits are 0	All bits are 1
Green	All bits are 0	All bits are 1	All bits are 0
Cyan	All bits are 0	All bits are 1	All bits are 1
Red	All bits are 1	All bits are 0	All bits are 0
Magenta	All bits are 1	All bits are 0	All bits are 1
Yellow	All bits are 1	All bits are 1	All bits are 0
White	All bits are 1	All bits are 1	All bits are 1

**Note:** There are only defined main colors on this table - Not all gray levels of colors.

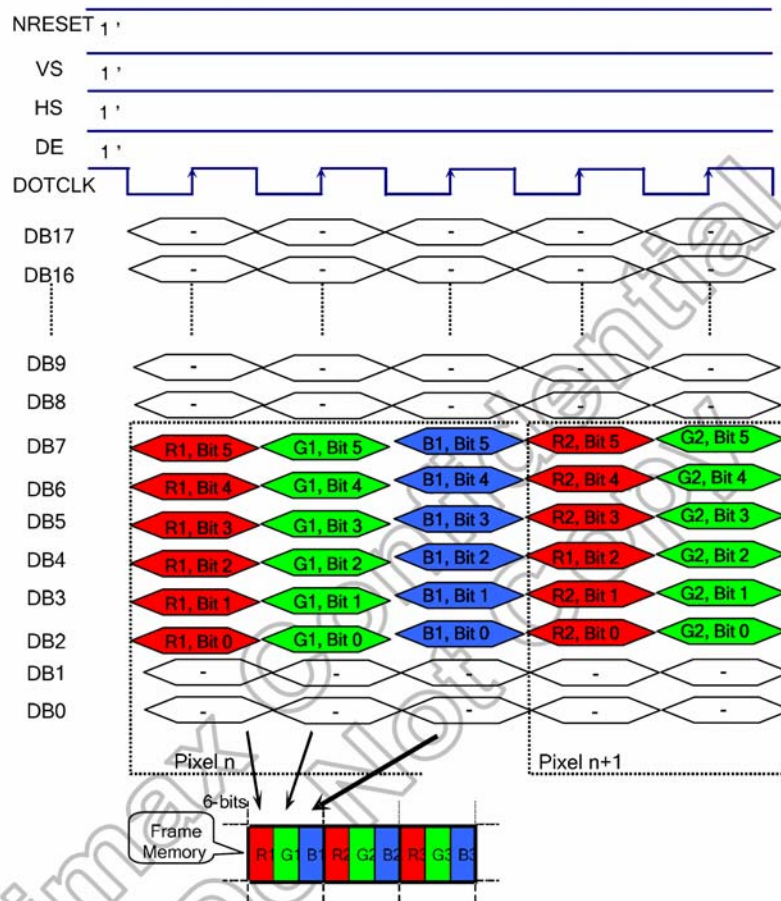
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## 7-11 RGB data color coding

18-bits/pixel Colors Order on 6-bit Data width RGB Interface (RGB 6-6-6-bit input).

There is 1 pixel (3 sub-pixels) per 3 bytes, 262K-colors, 17H="E0h"

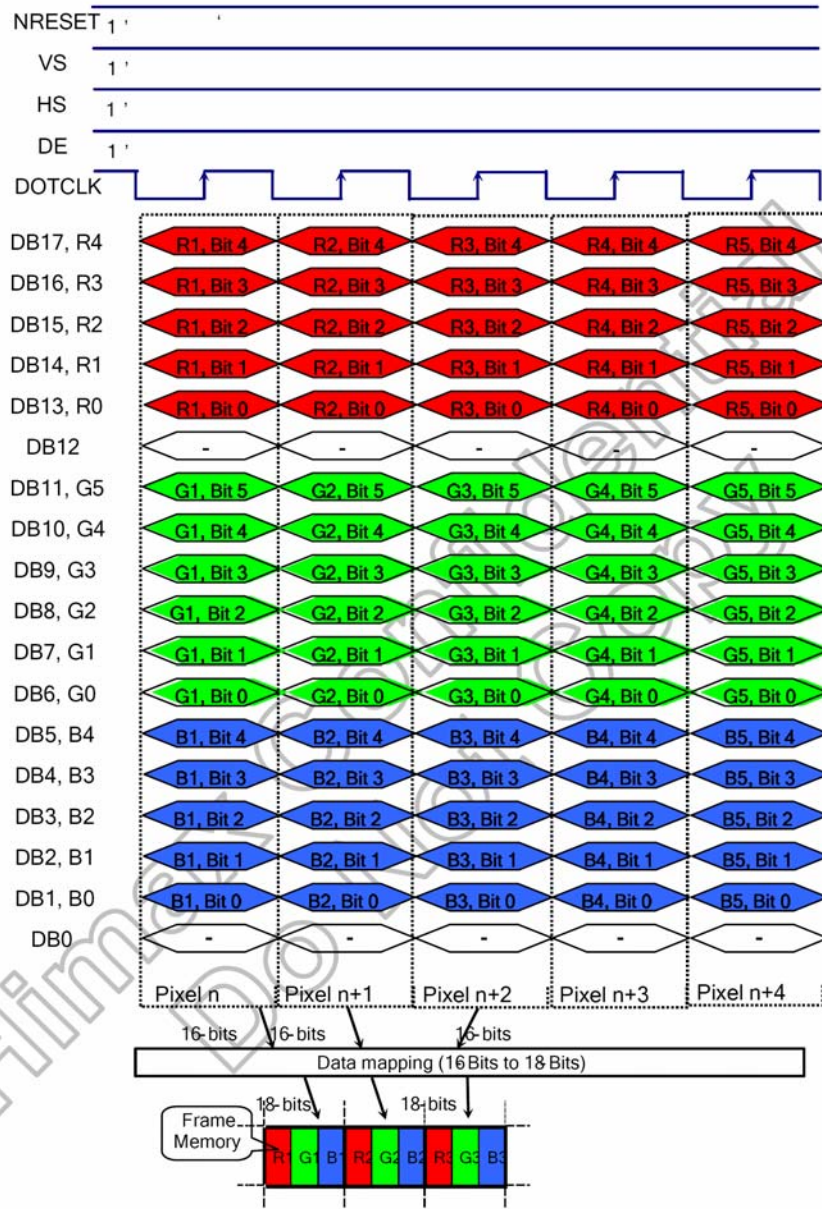


**Note:** (1) The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit7, LSB=Bit0 for Red, Green and Blue data. (3-transfer data one pixel)  
(2) '-' Don't care, but need to set IOVCC or VSSD level.

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16-bits/pixel Colors Order on the 16-bits Data width RGB Interface (RGB 5-6-5-bits input). There is 1 pixel (3 sub-pixels) per byte, 65K-colors, 17H="50h"



**Note:** (1) The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

(2) '-' Don't care, but need to set IOVCC or VSSD level.





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## 7-12 Instruction List

LCD Driver/Controller IC:HX8347-D

(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
00	Himax ID	R	-	0	1	0	0	0	1	1	1	-
01	Display Mode control	W/R	-	DP_S TB(0)	DP_STB S(0)	-	-	SCROL (0)	IDMON (0)	INVON (0)	PTLON (0)	-
02	Column address start 2	W/R	-	SC[15:8] (8'b0000_0000)								-
03	Column address start 1	W/R	-	SC[7:0] (8'b0000_0000)								-
04	Column address end 2	W/R	-	EC[15:8] (8'b0000_0000)								-
05	Column address end 1	W/R	-	EC[7:0] (8'b1110_1111)								-
06	Row address start 2	W/R	-	SP[15:8] (8'b0000_0000)								-
07	Row address start 1	W/R	-	SP[7:0] (8'b0000_0000)								-
08	Row address end 2	W/R	-	EP[15:8] (8'b0000_0001)								-
09	Row address end 1	W/R	-	EP[7:0] (8'b0011_1111)								-
0A	Partial area start row 2	W/R	-	PSL[15:8] (8'b0000_0000)								-
0B	Partial area start row 1	W/R	-	PSL[7:0] (8'b0000_0000)								-
0C	Partial area end row 2	W/R	-	PEL[15:8] (8'b0000_0001)								-
0D	Partial area end row 1	W/R	-	PEL[7:0] (8'b0011_1111)								-
0E	Vertical Scroll Top fixed area 2	W/R	-	TFA[15:8] (8'b0000_0000)								-
0F	Vertical Scroll Top fixed area 1	W/R	-	TFA[7:0] (8'b0000_0000)								-
10	Vertical Scroll height area 2	W/R	-	VSA[15:8] (8'b0000_0001)								-
11	Vertical Scroll height area 1	W/R	-	VSA[7:0] (8'b0100_0000)								-
12	Vertical Scroll Button area 2	W/R	-	BFA[15:8] (8'b0000_0000)								-
13	Vertical Scroll Button area 1	W/R	-	BFA [7:0] (8'b0000_0000)								-
14	Vertical Scroll Start address 2	W/R	-	VSP [15:8] (8'b0000_0000)								-
15	Vertical Scroll Start address 1	W/R	-	VSP [7:0] (8'b0000_0000)								-
16	Memory Access control	W/R	-	MY(0)	MX(0)	MV(0)	ML(0)	BGR(0)	-	-	-	-
17	COLMOD	W/R	-	CSEL[3:0] (4b'0110)				-	IFPF[2:0] (3b'110)			-
18	OSC Control 2	W/R	-	I/PI_RADJ1[3:0] (3b'0011)				N/P_RADJ0[3:0] (4b'0100)				-
19	OSC Control 1	W/R	-	-	-	-	-	-	-	-	OSC_EN(0)	-
1A	Power Control 1	W/R	-	-	-	-	-	-	BT[2:0] (001)			-
1B	Power Control 2	W/R	-	-	-	VRH[5:0] (01_1011)_4.8V						-
1C	Power Control 3	W/R	-	-	-	-	-	-	AP[2:0] (011)			-
1D	Power Control 4	W/R	-	-	I/PI_FS0[2:0] (100)			-	N/P_FS0[2:0] (100)			-
1E	Power Control 5	W/R	-	-	I/PI_FS1[2:0] (100)			-	N/P_FS1[2:0] (100)			-
1F	Power Control 6	W/R	-	GASEN(1)	VCOMG(0)	-	PON(0)	DK(1)	XDK(0)	DDVDH_TRI(0)	STB(1)	-
22	SRAM Write Control	W/R	-	SRAM Write								-
23	VCOM Control 1	W/R	-	VMF[7:0] (1000_0000)								-
24	VCOM Control 2	W/R	-	VMH[7:0] (0111_0001)								-
25	VCOM Control 3	W/R	-	VML[7:0] (0010_1111)								-
26	Display Control 1	W/R	-	-	-	-	-	ISC[3:0] (0001)				-
27	Display Control 2	W/R	-	PT[1:0] (10)		PTV[1:0] (10)		-	-	PTG(1)	REF(1)	-
28	Display Control 3	W/R	-	-	-	GON(1)	DTE(0)	D[1:0] (00)		-	-	-

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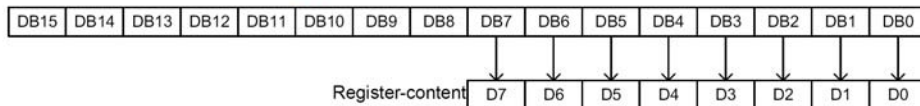
(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
29	Frame Rate control 1	W/R	-	I/PI_RTN[3:0](0010)				N/P_RTN[3:0](0010)				-
2A	Frame Rate Control 2	W/R	-	-	-	I/PI_DIV[1:0](00)	-	-	N/P_DIV[1:0](00)			-
2B	Frame Rate Control 3	W/R	-	N/P_DUM[7:0] (8b'0001_1100)								-
2C	Frame Rate Control 4	W/R	-	I/PI_DUM[7:0] (8b'0001_1100)								-
2D	Cycle Control 1	W/R	-	GDON[7:0] (8'b0000_1101)								-
2E	Cycle Control 2	W/R	-	GDOF[7:0] (8'b0111_0000)								-
2F	Display inversion	W/R	-	-	I/PI_NW[2:0](3b'001)			-	N/P_NW[2:0] (3b'001)			-
31	RGB interface control 1	W/R	-	-	-	-	-	-	-	RCM[1:0](00)		-
32	RGB interface control 2	W/R	-	-	-	-	-	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)	-
33	RGB interface control 3	W/R	-	HBP[7:0]								-
34	RGB interface control 4	W/R	-	HBP[9:8]			VBP[5:0]					-
36	Panel Characteristic	W/R	-	-	-	-	-	SS_P anel	GS_Pan el	REV_Pa nel	BGR_P anel	-
38	OTP Control 1	W/R	-	OTP_PTM[1:0]		OTP_VARDJ[1:0]		OTP_POR	OTP_OTPEN	OTP_PP ROG	OTP_P WE	-
39	OTP Control 2	W/R	-	-	-	-	-	-	OTP_Y A2	OTP_YA1	OTP_Y A0	-
3A	OTP Control 3	W/R	-	-	-	-	OTP_X A4	OTP_X A3	OTP_X A2	OTP_XA1	OTP_XA0	-
3C	CABC Control 1	W/R	-	DBV[7:0](8'h00)								-
3D	CABC Control 2	W/R	-	-	-	BCTRL (0)	-	DD (0)	BL (0)	-	-	-
3E	CABC Control 3	W/R	-	-	-	-	-	-	-	C1 (0)	C0 (0)	-
3F	CABC Control 4	W/R	-	CMB[7:0](8'h00)								-
40	r1 Control (1)	W/R	-	-	-	-	-	VRP0[5:0] (6'b00_0001)				-
41	r1 Control (2)	W/R	-	-	-	-	-	VRP1[5:0] (6'b00_1110)				-
42	r1 Control (3)	W/R	-	-	-	-	-	VRP2[5:0] (6'b01_0001)				-
43	r1 Control (4)	W/R	-	-	-	-	-	VRP3[5:0] (6'b01_1010)				-
44	r1 Control (5)	W/R	-	-	-	-	-	VRP4[5:0] (6'b01_1000)				-
45	r1 Control (6)	W/R	-	-	-	-	-	VRP5[5:0] (6'b10_0100)				-
46	r1 Control (7)	W/R	-	PRP0[6:0] (7'b001_0101)								-
47	r1 Control (8)	W/R	-	PRP1[6:0] (7'b110_0101)								-
48	r1 Control (9)	W/R	-	-	-	-	-	PKP0[4:0] (5'b0_1011)				-
49	r1 Control (10)	W/R	-	-	-	-	-	PKP1[4:0] (5'b1_100)				-
4A	r1 Control (11)	W/R	-	-	-	-	-	PKP2[4:0] (5'b1_1001)				-
4B	r1 Control (12)	W/R	-	-	-	-	-	PKP3[4:0] (5'b1_1010)				-
4C	r1 Control (13)	W/R	-	-	-	-	-	PKP4[4:0] (5'b1_1000)				-
50	r1 Control (14)	W/R	-	-	-	-	-	VRN0[5:0] (6'b01_1011)				-
51	r1 Control (15)	W/R	-	-	-	-	-	VRN1[5:0] (6'b10_0111)				-
52	r1 Control (16)	W/R	-	-	-	-	-	VRN2[5:0] (6'b10_0101)				-
53	r1 Control (17)	W/R	-	-	-	-	-	VRN3[5:0] (6'b10_1110)				-
54	r1 Control (18)	W/R	-	-	-	-	-	VRN4[5:0] (6'b11_0001)				-
55	r1 Control (19)	W/R	-	-	-	-	-	VRN5[5:0] (6'b11_1110)				-
56	r1 Control (20)	W/R	-	-	-	-	-	PRN0[6:0] (7'b001_1010)				-
57	r1 Control (21)	W/R	-	-	-	-	-	PRN1[6:0] (7'b110_1010)				-
58	r1 Control (22)	W/R	-	-	-	-	-	PKN0[4:0] (5'b0_0111)				-
59	r1 Control (23)	W/R	-	-	-	-	-	PKN1[4:0] (5'b0_0101)				-
5A	r1 Control (24)	W/R	-	-	-	-	-	PKN2[4:0] (5'b0_0110)				-
5B	r1 Control (25)	W/R	-	-	-	-	-	PKN3[4:0] (5'b0_1011)				-
5C	r1 Control (26)	W/R	-	-	-	-	-	PKN4[4:0] (5'b1_0100)				-
5D	r1 Control (27)	W/R	-	CGMN1[1:0] (11)		CGMN0[1:0](00)		CGMP1[1:0](11)		CGMP0[1:0](00)		-
60	TE Control	W/R	-	-	-	-	TE_mod e(0)	TEOE(0)		-	-	-
E4	Power saving 1	W/R	-	EQ_S1[7:0]								-
E5	Power saving 2	W/R	-	EQ_S2[7:0]								-
E6	Power saving 3	W/R	-	EQ_S3[7:0]								-
E7	Power saving 4	W/R	-	EQ_S4[7:0]								-
E8	Source OP control Normal	W/R	-	OPON_N[7:0]								-

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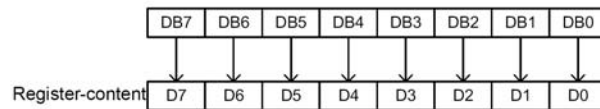
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(Hex)	Operation Code	W/R	Upper Code	Lower Code							Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0
E9	Source OP control_IDLE	W/R	-	OPON_I[7:0]							-
EA	Power control internal use (1)	W/R	-	STBA[15:8]							-
EB	Power control internal use (2)	W/R	-	STBA[7:0]							-
EC	Source control internal use (1)	W/R	-	PTBA[15:8]							-
ED	Source control internal use (2)	W/R	-	PTBA[7:0]							-
FF	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)	-

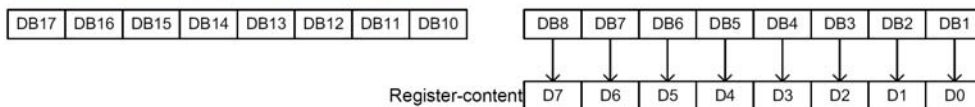
IM3~IM0 = "0000" 8080 MCU 16-bits Parallel type I



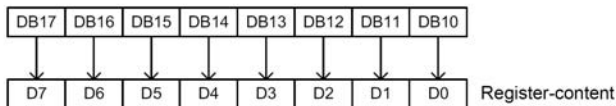
IM3~IM0 = "0001" 8080 MCU 8-bits Parallel type I



IM3~IM0 = "0010" 8080 MCU 16-bits Parallel type II



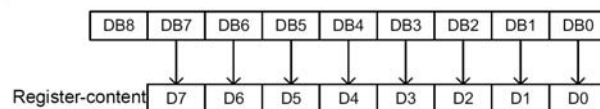
IM3~IM0 = "0011" 8080 MCU 8-bits Parallel type II



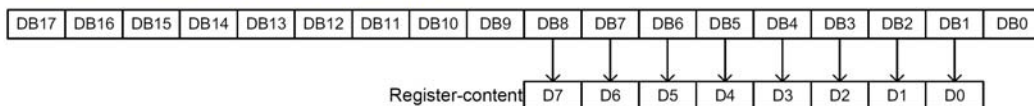
IM3~IM0 = "1000" 8080 MCU 18-bits Parallel type I



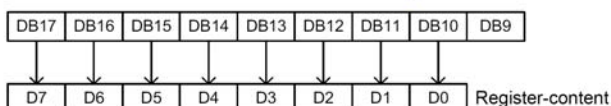
IM3~IM0 = "1001" 8080 MCU 9-bits Parallel type I



IM3~IM0 = "1010" 8080 MCU 18-bits Parallel type II



IM3~IM0 = "1011" 8080 MCU 9-bits Parallel type II



## Preliminary

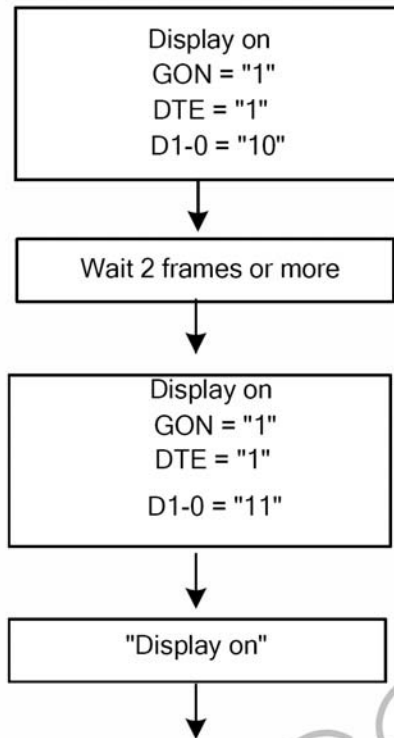
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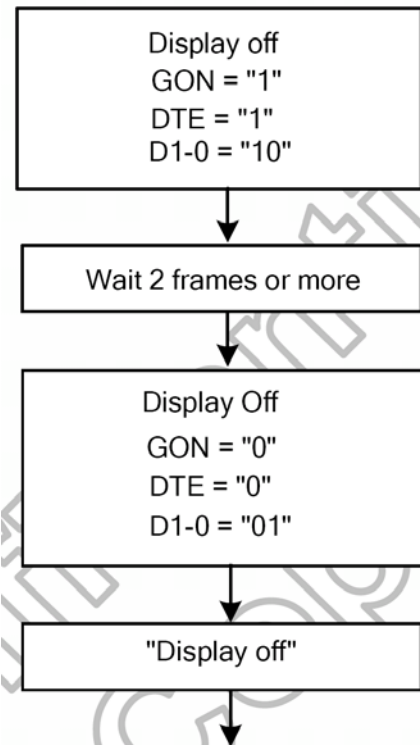
## 8 Application

### 8-1 Display ON / OFF

Display on flow



Display off flow



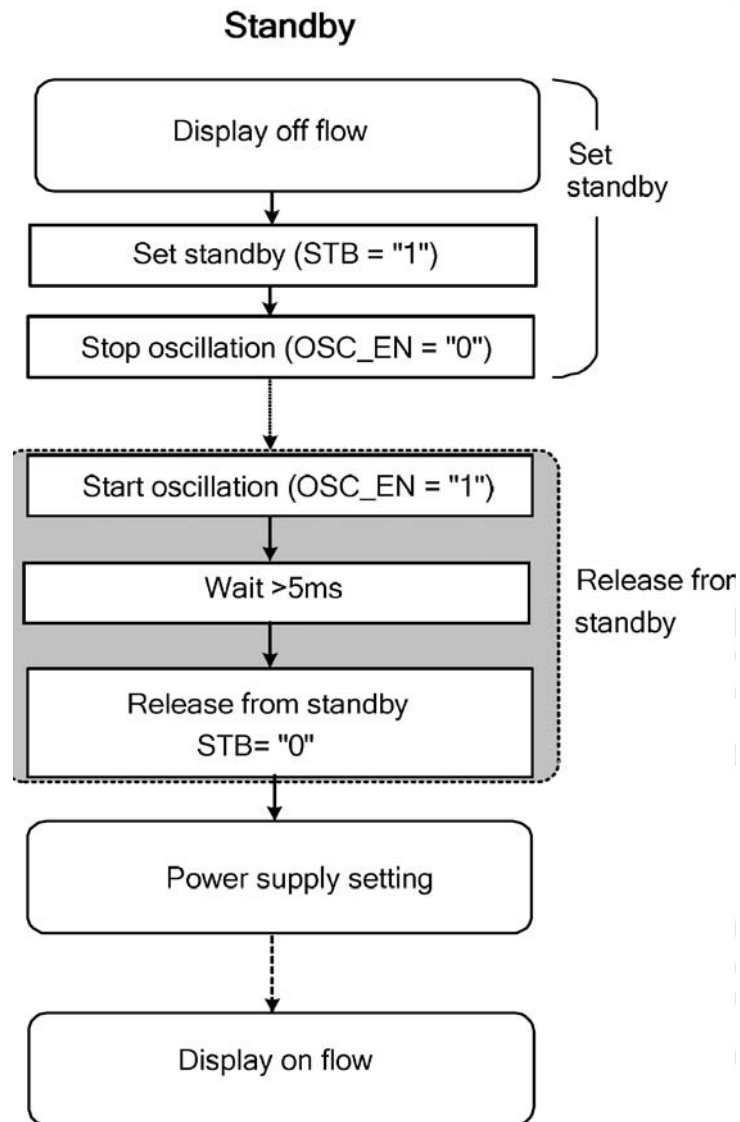


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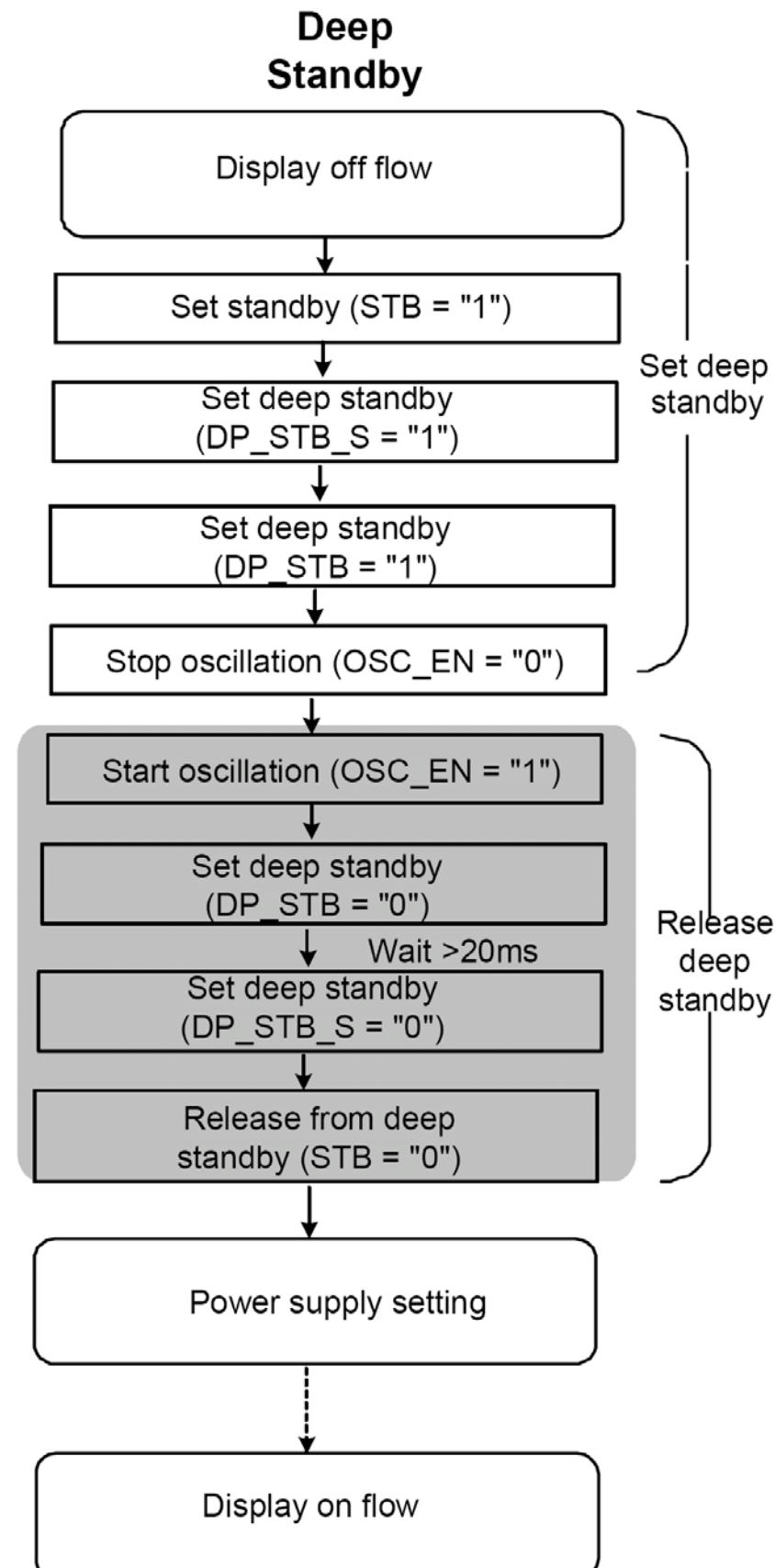
### 8-2 Standby mode



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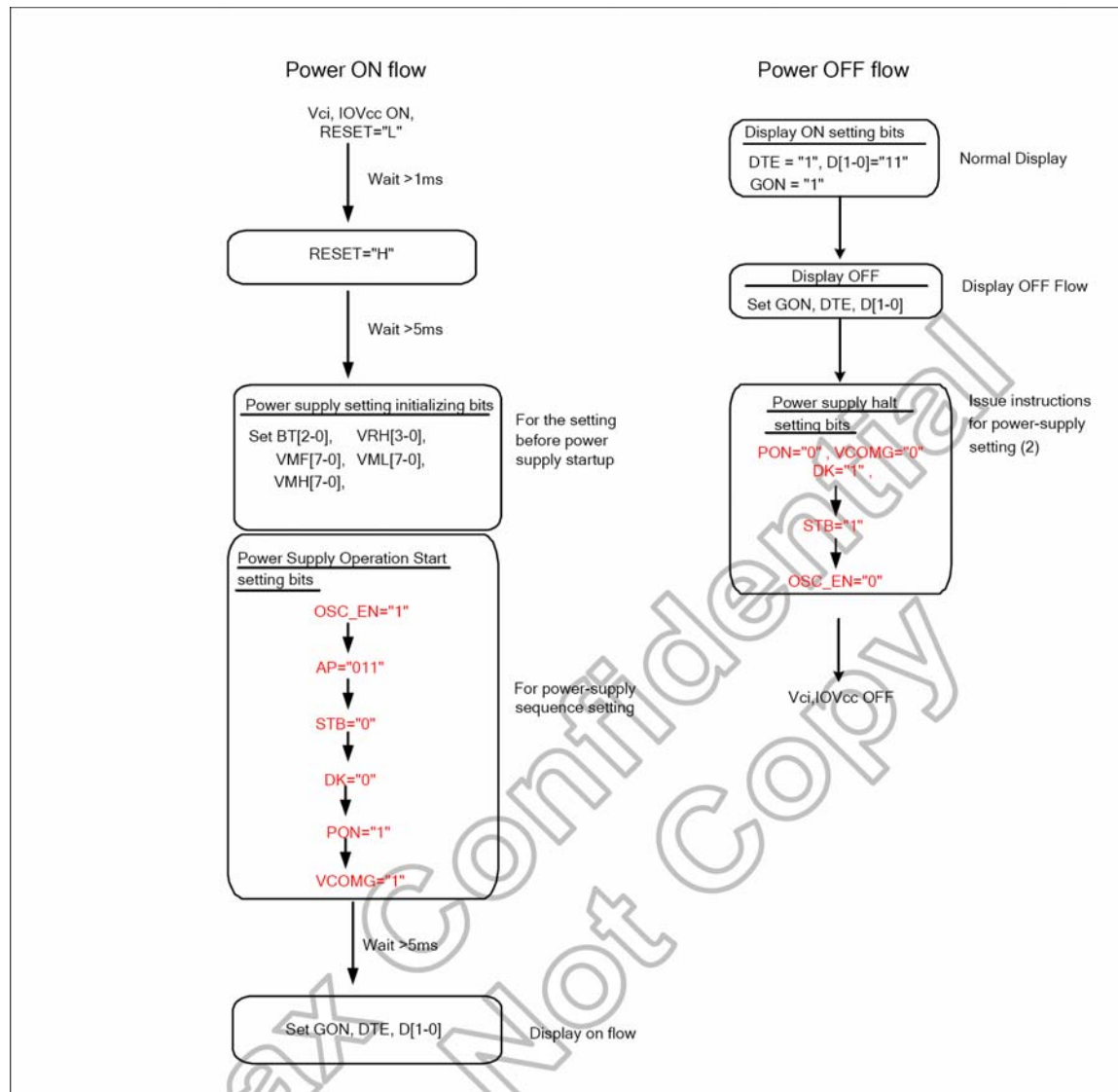
### 8-3 Deep Standby mode



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### 8-4 Power ON/OFF setting flow

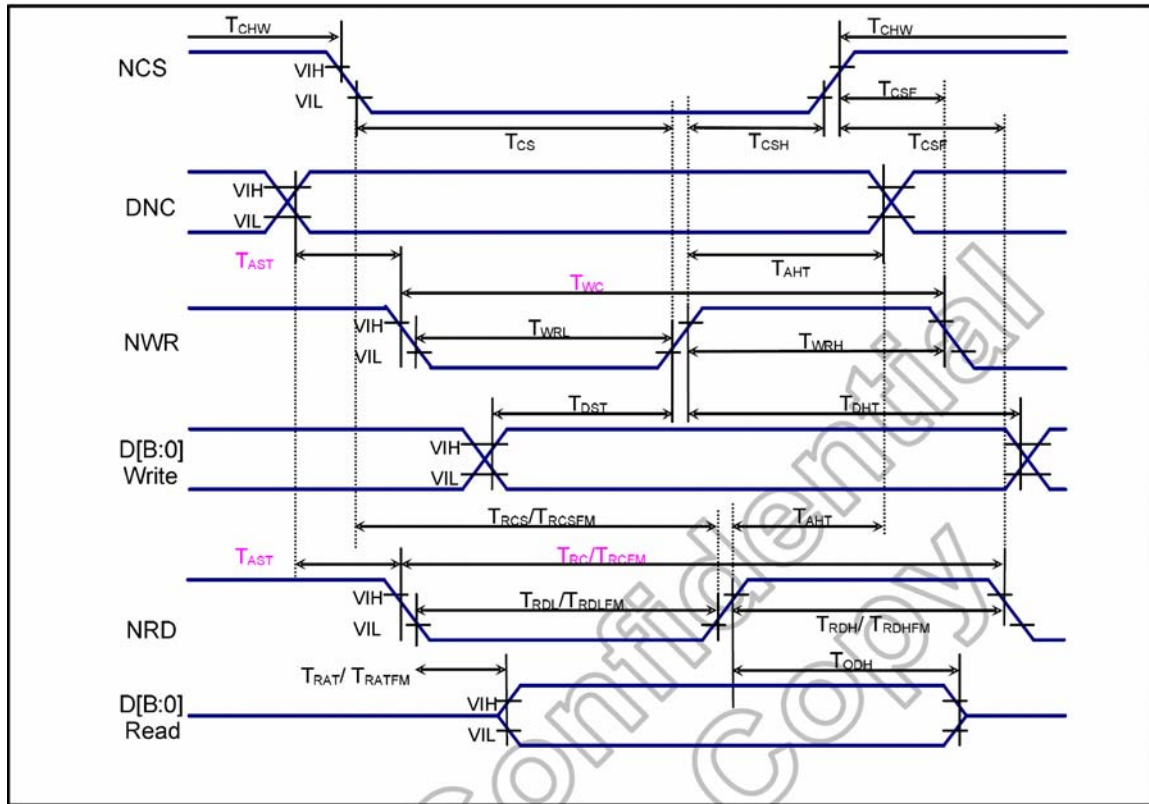


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# 9 Electrical Characteristics

## 9-1 AC Characteristics



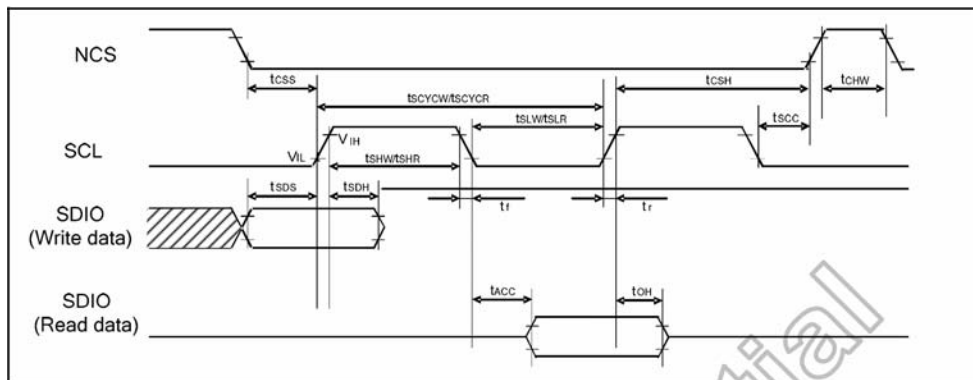
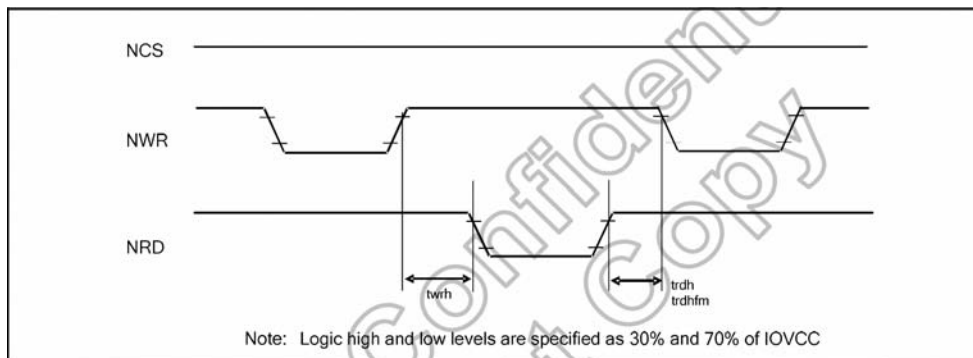
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T<sub>A</sub> = -30 to 70 ° C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	tAST	Address setup time	0	-	ns	-
	tAHT	Address hold time (Write/Read)	10	-	ns	-
NCS	tCHW	Chip select "H" pulse width	0	-	-	-
	tCS	Chip select setup time (Write)	15	-	-	-
	tRCS	Chip select setup time (Read ID)	45	-	ns	-
	tRCSFM	Chip select setup time (Read FM)	355	-	-	-
	tCSF	Chip select wait time (Write/Read)	10	-	-	-
	tCSH	Chip select hold time	10	-	-	-
NWR_SCL	tWC	Write cycle	66	-	-	-
	tWRH	Control pulse "H" duration	15	-	ns	-
	tWRL	Control pulse "L" duration	15	-	-	-
NRD(ID)	tRC	Read cycle (ID)	160	-	-	-
	tRDH	Control pulse "H" duration (ID)	90	-	ns	When read ID data
	tRDL	Control pulse "L" duration (ID)	45	-	-	-
NRD(FM)	tRCFM	Read cycle (FM)	450	-	-	-
	tRDHFM	Control pulse "H" duration (FM)	90	-	ns	When read from frame memory
	tRDLFM	Control pulse "L" duration (FM)	355	-	-	-
DB17 to DB0	tDST	Data setup time	10	-	-	-
	tDHT	Data hold time	10	-	-	-
	tRAT	Read access time (ID)	-	40	ns	For maximum CL=30pF
	tRATFM	Read access time (FM)	-	340	-	For minimum CL=8pF
	tODH	Output disable time	20	80	-	-

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

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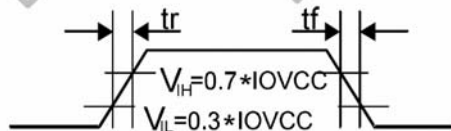
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T<sub>A</sub>=-30 to 70° C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write)	tSCYCW	SCL	20	-	-	ns
SCL "H" pulse width (Write)	tSHW		8	-	-	
SCL "L" pulse width (Write)	tSLW		8	-	-	
Data setup time (Write)	tSDS	SDIO	10	-	-	ns
Data hold time (Write)	tSDH		10	-	-	
Serial clock cycle (Read)	tSCYCR	SCL	150	-	-	ns
SCL "H" pulse width (Read)	tSHR		60	-	-	
SCL "L" pulse width (Read)	tSLR		60	-	-	
Access Time	tACC	SDI for maximum CL=30pF For minimum CL=8pF	10	-	50	ns
Output disable time	tOH	SDO For maximum CL=30pF For minimum CL=8pF	15	-	50	ns
SCL to Chip select	tSCC	SCL, NCS	20	-	-	ns
NCS "H" pulse width	tCHW	NCS	40	-	-	ns
Chip select setup time	tCSS	NCS	15	-	-	ns
Chip select hold time	tCSH		15	-	-	

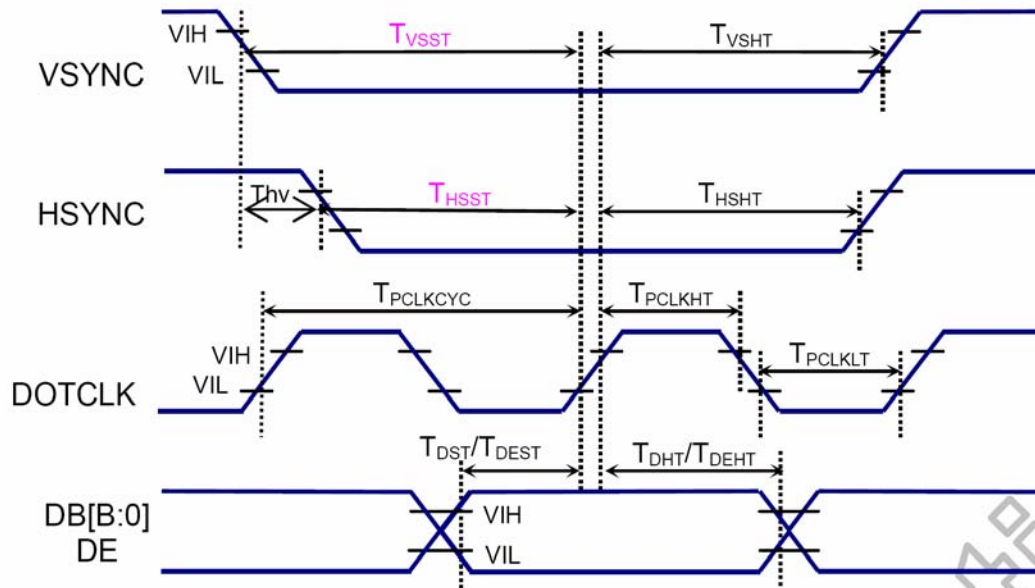
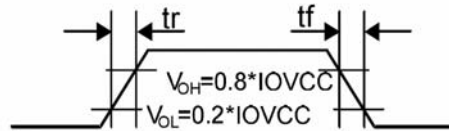
**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

### Input Signal Slope



### Output Signal Slope





## Preliminary

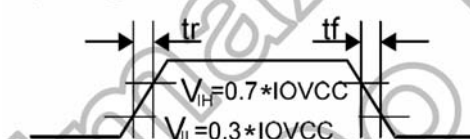
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(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -30 to 70 ° C)

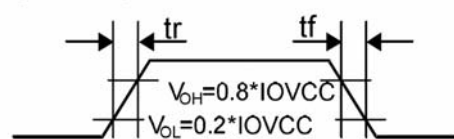
Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Pixel low pulse width	$T_{CLKLT}$	-	15	-	-	ns
Pixel high pulse width	$T_{CLKHT}$	-	15	-	-	ns
Vertical Sync. set-up time	$T_{VSST}$	-	15	-	-	ns
Vertical Sync. hold time	$T_{VSSH}$	-	15	-	-	ns
Horizontal Sync. set-up time	$T_{HSST}$	-	15	-	-	ns
Horizontal Sync. hold time	$T_{HSSH}$	-	15	-	-	ns
Data Enable set-up time	$T_{DEST}$	-	15	-	-	ns
Data Enable hold time	$T_{DEHT}$	-	15	-	-	ns
Data set-up time	$T_{DST}$	-	15	-	-	ns
Data hold time	$T_{DHT}$	-	15	-	-	ns
Phase difference of sync signal falling edge	Thv	-	0	-	240	Dotclk

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

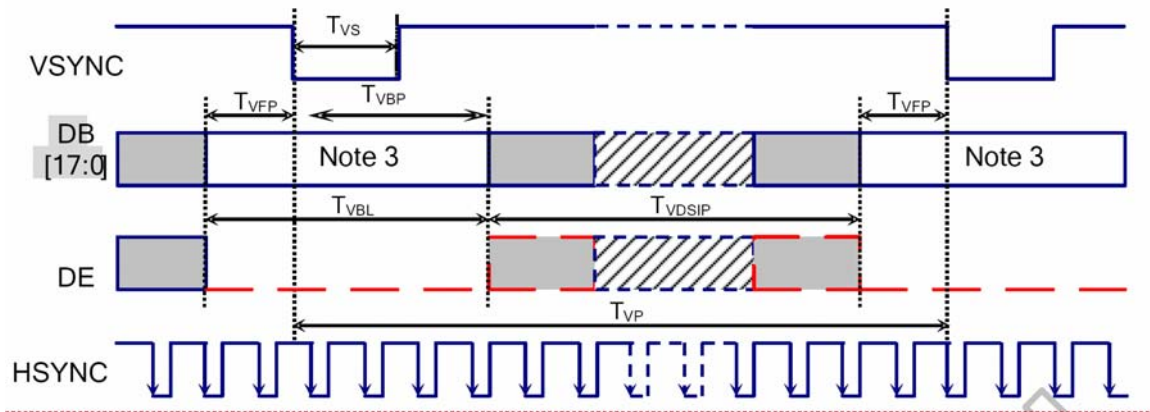
### Input Signal Slope



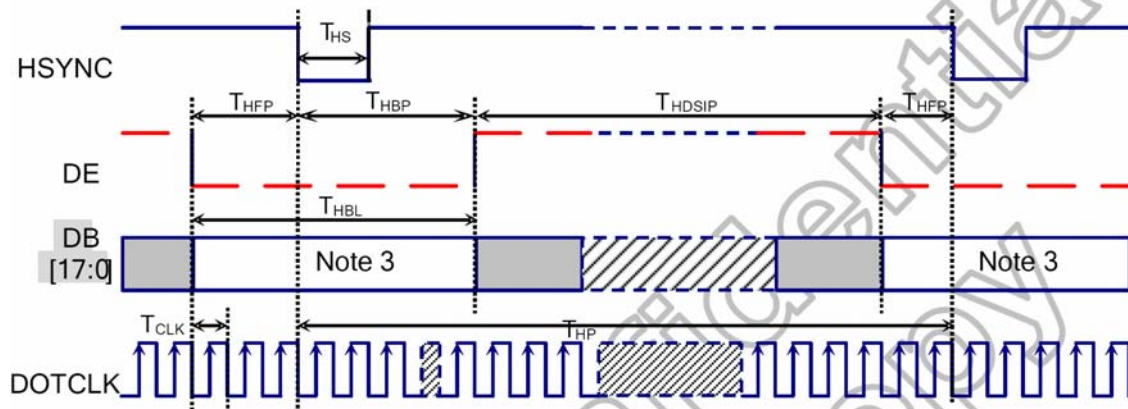
### Output Signal Slope



### Vertical Timing for RGB I/F



### Horizontal Timing for RGB I/F





## Preliminary

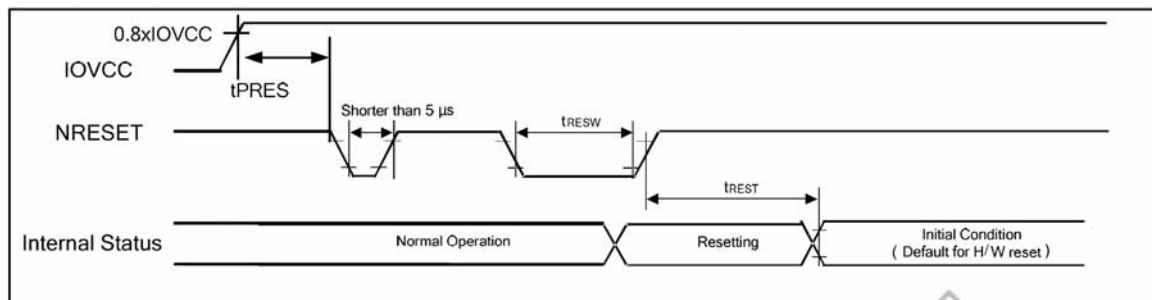
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Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical Timing						
Vertical cycle period	T <sub>VP</sub>	-	324	326	452	HS
Vertical low pulse width	T <sub>VS</sub>	-	2	2	-	HS
Vertical front porch	T <sub>VFP</sub>	-	2	2	6	HS
Vertical back porch	T <sub>VBP</sub>	-	2	4	126	HS
Vertical blanking period	T <sub>VBL</sub>	T <sub>VBP</sub> + T <sub>VFP</sub>	4	6	132	HS
Vertical active area	T <sub>VDISP</sub>	-	-	320	-	HS
			-		-	HS
			-		-	HS
Vertical refresh rate	TVRR	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T <sub>HP</sub>	-	244	252	1008	DOTCLK
Horizontal low pulse width	T <sub>HS</sub>	-	2	2	256	DOTCLK
Horizontal front porch	T <sub>HFP</sub>	-	2	4	256	DOTCLK
Horizontal back porch	T <sub>HBP</sub>	-	2	8	256	DOTCLK
Horizontal blanking period	T <sub>HBL</sub>	T <sub>HBP</sub> + T <sub>HFP</sub>	4	12	256	DOTCLK
Horizontal active area	T <sub>HDISP</sub>	-	-	240	-	DOTCLK
Pixel clock cycle TVRR=60Hz	f <sub>CLKCYC</sub>	-	3.9	-	16.6	MHz

**Note:** (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V,  $T_A$ =-30 to 70°C (to +85°C no damage)

(2) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(3) HP is multiples of DOTCLK.



Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width <sup>(1)</sup>	NRESET	10	-	-	-	μs
tREST	Reset complete time <sup>(2)</sup>	-	-	-	5	When reset applied during STB OUT mode	ms
		-	-	-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

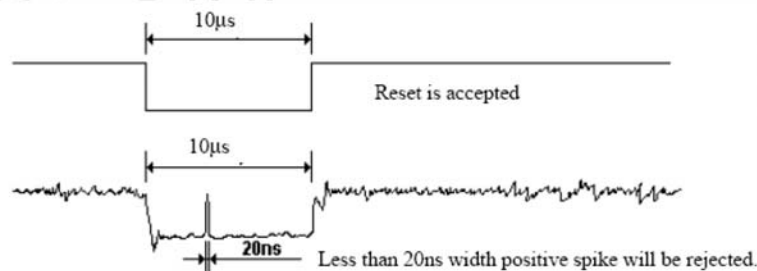
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**Note:** (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 $\mu$ s	Reset Rejected
Longer than 10 $\mu$ s	Reset
Between 5 $\mu$ s and 10 $\mu$ s	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, VMF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time ( $t_{REST}$  within 5ms after a rising edge of NRESET).
- (4) Spike Rejection also applies during a valid reset pulse as shown below:



- (5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out

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# **10 QUALITY AND RELIABILITY**

## **1. Scope**

Specifications contain

1.1 Display Quality Evaluation

1.2 Mechanics Specification

## **2. Sampling Plan**

Unless there is other agreement, the sampling plan for incoming inspection shall

follow MIL-STD-105E LEVEL II.

2.1 Lot size: Quantity per shipment as one lot (different model as different lot ).

2.2 Sampling type: Normal inspection, single sampling.

2.3 Sampling level: Level II.

2.4 AQL: Acceptable Quality Level

Major defect: AQL=0.65

Minor defect: AQL=1.0

## **3. Panel Inspection Condition**

3.1 Environment:

Room Temperature:  $25\pm 5^{\circ}\text{C}$ .

Humidity:  $65\pm 5\%$  RH.

Illumination: 300 ~ 700 Lux.

3.2 Inspection Distance:

35-40 cm

3.3 Inspection Angle:

The vision of inspector should be perpendicular to the surface of the Module.

3.4 Inspection time :

Perceptibility Test Time: 20 seconds max.

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### 4. Display Quality

#### 4.1 Function Related:

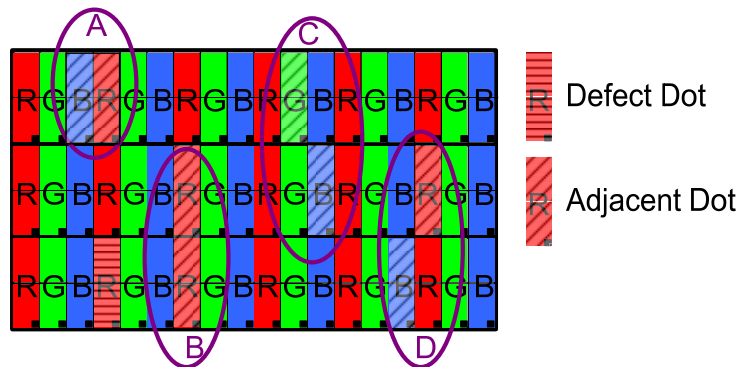
The function defects of line defect, abnormal display, and no display are considered Major defects.

#### 4.2 Bright/Dark Dots:

Defect Type / Specification	G0 Grade	A Grade
Bright Dots	0	$N \leq 2$
Dark Dots	0	$N \leq 3$
Total Bright and Dark Dots	0	$N \leq 4$

#### [Note 1]

Judge defect dot and adjacent dot as following.



- (1) One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)
- (2) The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
- (3) Allow above (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2 defect dots in total quantity.
- (4) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.
- (5) There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

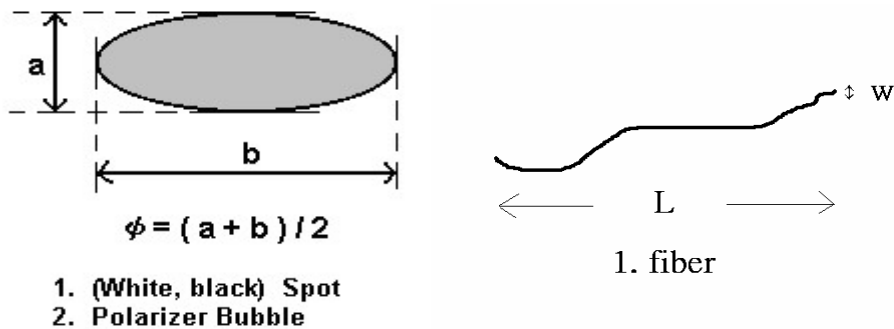
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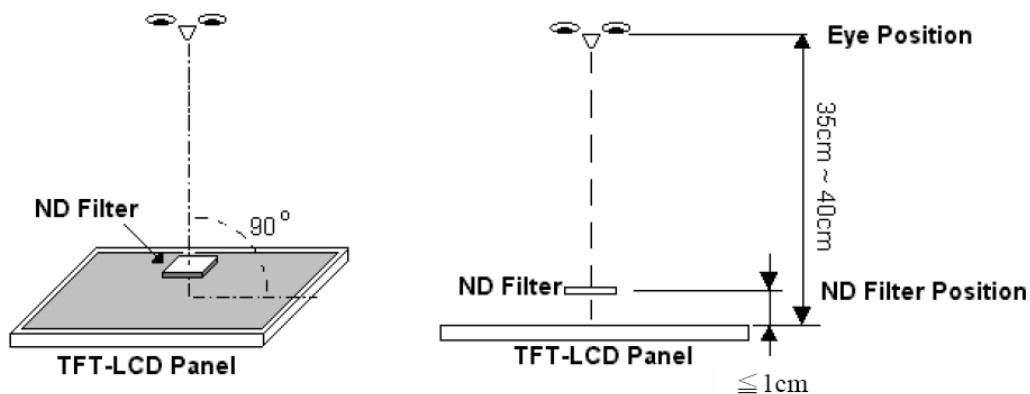
### 4.3 Visual Inspection specifications:

Defect Type	Specification	Count(N)
Dot Shape (Particle, Scratch and Bubbles in display area)	$D \leq 0.2\text{mm}$	Ignored
	$0.2\text{mm} < D \leq 0.4\text{mm}$	$N \leq 3$
	$D > 0.4\text{mm}$	$N=0$
Line Shape (Particles, Scratch, Lint and Bubbles in display area)	$W \leq 0.05\text{mm}$	Ignored
	$0.05\text{mm} < W \leq 0.1\text{mm}$ , $L \leq 4\text{mm}$	$N \leq 3$
	$W > 0.1\text{mm}$ , $L > 4\text{mm}$	$N=0$

[Note 2] W : Width[mm], L : Length[mm], N : Number,  $\phi$  : Average Diameter



[Note 3] Bright dot is defined through 6% transmission ND Filter as following.



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**5 Reliability Test**

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	80±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 m in. 5 min. 30 min. ( 1 cycle ) Total 5 cycle	1,2
Humidity Test	60 °C, Humidity 90%, 96 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions  
(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

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# **11 USE PRECAUTIONS**

## **11-1 Handling precautions**

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

## **11-2 Installing precautions**

- 1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx.  $1M\Omega$  and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.



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### 11-3 Storage precautions

- 1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

### 11-4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- 3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- 7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

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- 8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

**11-5 Other**

- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
- 3) AMIPRE will provide one years warrantee for all products and three months warrantee for all repairing products.

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**Top View Dimensions:**

- Overall width: 85.5±1.0
- LED pitch: 61.5±0.2 (LED)
- LED width: 4.03±0.2 (LCD)
- LED height: 4.36±0.2 (LED)
- LED spacing: 36.72 (A,A)
- LED width (A,A): 48.96 (A,A)
- LED spacing (A,A): 52.46±0.2 (LCD)
- LED width (A,A): 56.26±0.2 (LCD)
- LED height (A,A): 4.03±0.2 (LCD)
- LED spacing (A,A): 36.72 (A,A)
- LED width (A,A): 48.96 (A,A)
- LED spacing (A,A): 52.46±0.2 (LCD)
- LED width (A,A): 56.26±0.2 (LCD)

**Back View Dimensions:**

- Overall width: 85.5±1.0
- LED pitch: 61.5±0.2 (LED)
- LED width: 4.03±0.2 (LCD)
- LED height: 4.36±0.2 (LED)
- LED spacing: 36.72 (A,A)
- LED width (A,A): 48.96 (A,A)
- LED spacing (A,A): 52.46±0.2 (LCD)
- LED width (A,A): 56.26±0.2 (LCD)
- LED height (A,A): 4.03±0.2 (LCD)
- LED spacing (A,A): 36.72 (A,A)
- LED width (A,A): 48.96 (A,A)
- LED spacing (A,A): 52.46±0.2 (LCD)
- LED width (A,A): 56.26±0.2 (LCD)

**Pinout Table:**

1	ENABLE	27	PD15(R3)
2	DOTCLK	28	PD16(R4)
3	HSYNC	29	PD17(R5)
4	VSNC	30	VDD
5	/CS	31	VCI
6	WR/SCL	32	VCI
7	SDI	33	NC
8	RS	34	NC
9	NC	35	NC
10	/RD	36	NC
11	/RESRT	37	NC
12	PD0(B0)	38	NC
13	PD1(B1)	39	NC
14	PD2(B2)	40	GND
15	PD3(B3)	41	NC
16	PD4(B4)	42	NC
17	PD5(B5)	43	NC
18	PD6(G0)	44	NC
19	PD7(G1)	45	GND
20	PD8(G2)	46	SP0
21	PD9(G3)	47	NC
22	PD10(G4)	48	NC
23	PD11(G5)	49	NC
24	PD12(R0)	50	GND
25	PD13(R1)	51	GND
26	PD14(R2)		