



TRC101/102

FHSS

By

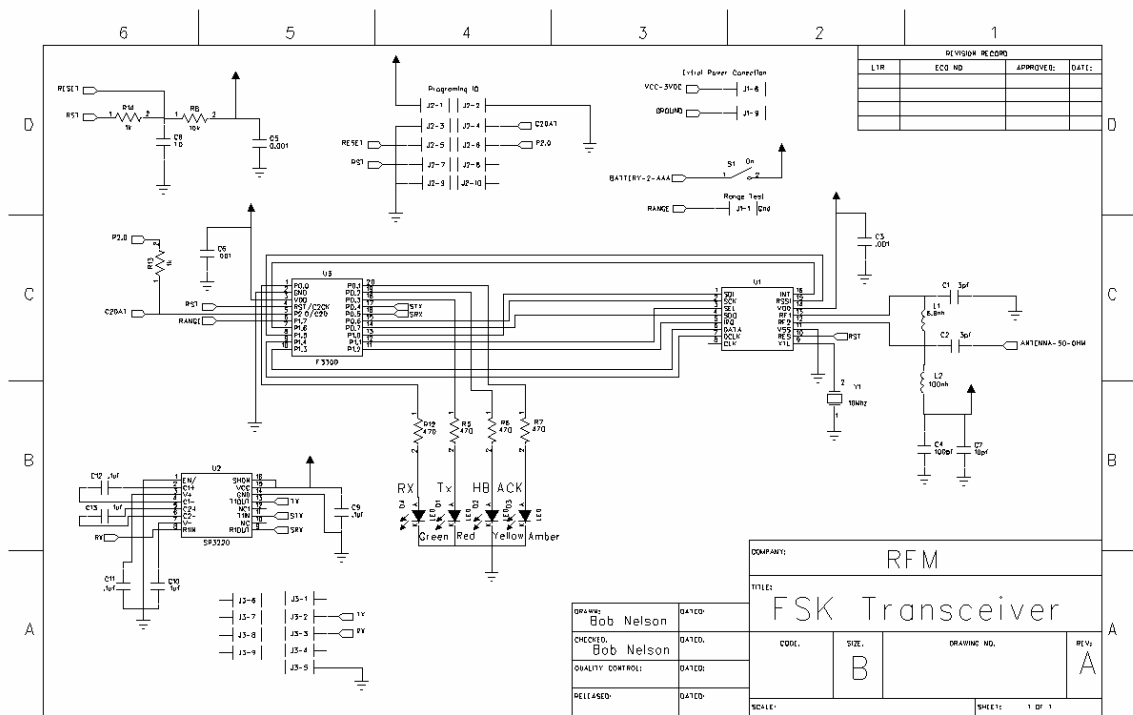
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Scope:

This application will demonstrate the ease of implementing a FHSS radio when using the TRC101/2. This document will give you the schematic and firmware to implement the design. Keep in mind that the TRC101/2 will meet or exceed FCC 15.249 power requirements and this application note is intended to use the higher power out while the radio is being used has a FHSS mode meeting FCC 15.247 rules and regulations.

Schematic:



Theory:

According to FCC 15.247 rules, the transmitter can not dwell on any giver channel longer than 400ms. Also the FCC requires you to hop to at least 25 channels during your operation.

The firmware below uses the TRC101/102 RFIC to accomplish this with ease do to the fast channel switching time within the transceiver (13us or faster). The firmware is sending a short range test packet which you can modify to add your data. During operation the channel that the transmitter is going to switch to will follow the packet number being sent within the packet protocol to make the synchronization simple and fast.

The micro that is used in this demo is the Silabs 330F utilizing the internal clock oscillator.

Firmware:

A51 MACRO ASSEMBLER TRC101/102FH

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MACRO ASSEMBLER A51 V7.04a
OBJECT MODULE PLACED IN CSL_330-trc101fh.OBJ
ASSEMBLER INVOKED BY: C:\SiLabs\MCU\IDEfiles\C51\BIN\a51.exe CSL_330-trc101fh.asm XR GEN DB EP NOMOD51

```
LOC OBJ          LINE    SOURCE
1                ;*****
2                ;          TRC101 FSK FHSS 25 Channel Range Test
3                ;          Running in Analog Mode
4                ;          Using RFM Symbols(although its not needed)
5                ;          RS232 running at 19.2
6                ;          RF Data Rate = 22.6Kbps raw
7                ;          Reciever Bandwidth = 200Khz
8                ;          Trtansmitter Dev. is 105Khz
9                ;          Range test data = "FHSS Test" plus pre-amble and CRC16 at the end
10               ;
11               ;*****
12               ;
13               ;          CSL_330-trc101fh.ASM
14               ;
15               ;          Range Test Enabled when Jumper is installed
16               ;          Jumper is only read at power up
17               ;
18               ;          D1 LED = RX          (White)
19               ;          D2 LED = TX          (RED)
20               ;          D3 LED = HB          (Amber)
21               ;          D4 LED = TX ACK     (Yellow)
22               ;
23               ;          Experimental software - NO representation is
24               ;          made that this software is suitable for any purpose
25               ;          Copyright(c) 2000 - 2007, RF Monolithics, Inc.
26               ;          SiLabs 8051C330 assembler source code file
27               ;          Low signal-to-noise protocol for RFM ASH transceiver
28               ;          type byte added, host & RF commands added
29               ;
30               ;
31               ;          This software provides physical
32               ;          layer control of a 2nd generation
33               ;          ASH transceiver, an OSI data link layer communication utility, an
34               ;          interface to a host computer through a UART port, and examples of
35               ;          command processing for RF network related messages and application
36               ;          related messages.
37               ;
38               ;          The software architecture includes two major components, a main
39               ;          loop which calls subroutines based on state flags, and an
40               ;          interrupt service routine (ISR) that is called by a timer.
41               ;
42               ;          The ISR handles real time processes such as RF transmission bit
43               ;          stream generation, clock and data recovery from a received RF bit
44               ;          stream, packet start vector detection, symbol framing of received
45               ;          message bits, running timers such as transmit retry timers, etc.
46               ;          The ISR tick rate is three times the bit rate for RF transmissions
47               ;          in this code version. (Four to eight ticks per bit are used in other
48               ;          versions.)
49               ;
50               ;          The main loop calls subroutines that load the transmit buffer, generate
51               ;          FCS error detection bits, initiate a message transmission, load the
52               ;          receive buffer, test FCS bits, generate ACKs, check packet addressees,
53               ;          service the hardware UART that communicates with the host, process
54               ;          commands received from the host or RF link, etc.
55               ;
56               ;          The subroutine called from the main loop that feeds symbols to the ISR
57               ;          for transmission and the subroutine that gets received symbols from
58               ;          the ISR are tightly synchronized using flags set by the ISR. Also, the
```

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59 ; timeout on messages received from the host (UART) are synchronized by
60 ; the ISR. Other main loop subroutines do not require tight synchronization
61 ; to the ISR.
62
63 ; The ISR always runs and can interrupt the main loop and any subroutine
64
65 ; the main loop calls. From the main loop's point of view, the ISR can
66 ; change the value of certain flags and certain byte buffers at any time.
67 ; The main loop and all related subroutines must be developed with this
68 ; in mind.
69
70 ; The tick ISR is never interrupted by any other process. However,
71 ; parts of the ISR can be activated or idled by state flags set/reset
72 ; by main loop subroutines. Also, the ISR shares data with main loop
73 ; using several common buffers.
74
75 ;$include (c8051f330.inc) ; SiLabs 8051C330 include file
+1 76 ;-----
+1 77 ;
+1 78 ;
+1 79 ;
+1 80 ;
+1 81 ; FILE NAME: C8051F330.INC
+1 82 ; TARGET MCUs: C8051F330, F331
+1 83 ; DESCRIPTION: Register/bit definitions for the C8051F330 product family.
+1 84 ;
+1 85 ; REVISION 1.0
+1 86 ;
+1 87 ;-----
+1 88
+1 89 ;REGISTER DEFINITIONS
+1 90 ;
0080 +1 91 P0          DATA 080H ; PORT 0 LATCH
0081 +1 92 SP          DATA 081H ; STACK POINTER
0082 +1 93 DPL        DATA 082H ; DATA POINTER LOW
0083 +1 94 DPH        DATA 083H ; DATA POINTER HIGH
0087 +1 95 PCON       DATA 087H ; POWER CONTROL
0088 +1 96 TCON       DATA 088H ; TIMER/COUNTER CONTROL
0089 +1 97 TMOD       DATA 089H ; TIMER/COUNTER MODE
008A +1 98 TLO        DATA 08AH ; TIMER/COUNTER 0 LOW
008B +1 99 TL1        DATA 08BH ; TIMER/COUNTER 1 LOW
008C +1 100 TH0       DATA 08CH ; TIMER/COUNTER 0 HIGH
008D +1 101 TH1       DATA 08DH ; TIMER/COUNTER 1 HIGH
008E +1 102 CKCON     DATA 08EH ; CLOCK CONTROL
008F +1 103 PSCCTL    DATA 08FH ; PROGRAM STORE R/W CONTROL
0090 +1 104 P1         DATA 090H ; PORT 1 LATCH
0091 +1 105 TMR3CN     DATA 091H ; TIMER/COUNTER 3 CONTROL
0092 +1 106 TMR3RL    DATA 092H ; TIMER/COUNTER 3 RELOAD CONTROL
0093 +1 107 TMR3RLH   DATA 093H ; TIMER/COUNTER 3 RELOAD HIGH
0094 +1 108 TMR3L      DATA 094H ; TIMER/COUNTER 3 LOW
0095 +1 109 TMR3H     DATA 095H ; TIMER/COUNTER 3 HIGH
0096 +1 110 IDA0L    DATA 096H ; CURRENT MODE DAC0 LOW
0097 +1 111 IDA0H    DATA 097H ; CURRENT MODE DAC0 HIGH
0098 +1 112 SCON0     DATA 098H ; UART0 CONTROL
0099 +1 113 SBUF0     DATA 099H ; UART0 DATA BUFFER
009B +1 114 CPT0CN     DATA 09BH ; COMPARATOR0 CONTROL
009D +1 115 CPT0MD     DATA 09DH ; COMPARATOR0 MODE SELECTION
009F +1 116 CPT0MX     DATA 09FH ; COMPARATOR0 MUX SELECTION
00A0 +1 117 P2         DATA 0A0H ; PORT 2 LATCH
00A1 +1 118 SPI0CFG     DATA 0A1H ; SPI CONFIGURATION
00A2 +1 119 SPI0CKR    DATA 0A2H ; SPI CLOCK RATE CONTROL
00A3 +1 120 SPI0DAT    DATA 0A3H ; SPI DATA
00A4 +1 121 P0MDOUT     DATA 0A4H ; PORT 0 OUTPUT MODE CONFIGURATION
00A5 +1 122 P1MDOUT     DATA 0A5H ; PORT 1 OUTPUT MODE CONFIGURATION
00A6 +1 123 P2MDOUT     DATA 0A6H ; PORT 2 OUTPUT MODE CONFIGURATION
00A8 +1 124 IE         DATA 0A8H ; INTERRUPT ENABLE

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00A9      +1 125 CLKSEL      DATA 0A9H ; CLOCK SELECT
00AA      +1 126 EMI0CN     DATA 0AAH ; EXTERNAL MEMORY INTERFACE CONTROL
00B1      +1 127 OSCXCN     DATA 0B1H ; EXTERNAL OSCILLATOR CONTROL
00B2      +1 128 OSCICN     DATA 0B2H ; INTERNAL OSCILLATOR CONTROL
00B3      +1 129 OSCICL     DATA 0B3H ; INTERNAL OSCILLATOR CALIBRATION
00B6      +1 130 FLSCL      DATA 0B6H ; FLASH SCALE
00B7      +1 131 FLKEY      DATA 0B7H ; FLASH LOCK AND KEY
00B8      +1 132 IP         DATA 0B8H ; INTERRUPT PRIORITY
00B9      +1 133 IDA0CN     DATA 0B9H ; CURRENT MODE DAC0 CONTROL
00BA      +1 134 AMXON      DATA 0BAH ; AMUX0 NEGATIVE CHANNEL SELECT
00BB      +1 135 AMXOP      DATA 0BBH ; AMUX0 POSITIVE CHANNEL SELECT
00BC      +1 136 ADC0CF     DATA 0BCH ; ADC0 CONFIGURATION
00BD      +1 137 ADC0L      DATA 0BDH ; ADC0 LOW
00BE      +1 138 ADC0H      DATA 0BEH ; ADC0 HIGH
00C0      +1 139 SMB0CN     DATA 0C0H ; SMBUS CONTROL
00C1      +1 140 SMB0CF     DATA 0C1H ; SMBUS CONFIGURATION
00C2      +1 141 SMB0DAT     DATA 0C2H ; SMBUS DATA
00C3      +1 142 ADC0GTL     DATA 0C3H ; ADC0 GREATER-THAN COMPARE LOW
00C4      +1 143 ADC0GTH     DATA 0C4H ; ADC0 GREATER-THAN COMPARE HIGH
00C5      +1 144 ADC0LTH     DATA 0C5H ; ADC0 LESS-THAN COMPARE WORD LOW
00C6      +1 145 ADC0LTH     DATA 0C6H ; ADC0 LESS-THAN COMPARE WORD HIGH
00C8      +1 146 TMR2CN     DATA 0C8H ; TIMER/COUNTER 2 CONTROL
00CA      +1 147 TMR2RL     DATA 0CAH ; TIMER/COUNTER 2 RELOAD LOW
00CB      +1 148 TMR2RLH    DATA 0CBH ; TIMER/COUNTER 2 RELOAD HIGH
00CC      +1 149 TMR2L      DATA 0CCH ; TIMER/COUNTER 2 LOW
00CD      +1 150 TMR2H      DATA 0CDH ; TIMER/COUNTER 2 HIGH
00D0      +1 151 PSW        DATA 0D0H ; PROGRAM STATUS WORD
00D1      +1 152 REF0CN     DATA 0D1H ; VOLTAGE REFERENCE CONTROL
00D4      +1 153 POSKIP     DATA 0D4H ; PORT 0 SKIP
00D5      +1 154 PLSKIP     DATA 0D5H ; PORT 1 SKIP
00D8      +1 155 PCA0CN     DATA 0D8H ; PCA CONTROL
00D9      +1 156 PCA0MD     DATA 0D9H ; PCA MODE
00DA      +1 157 PCA0CPM0    DATA 0DAH ; PCA MODULE 0 MODE REGISTER
00DB      +1 158 PCA0CPM1    DATA 0DBH ; PCA MODULE 1 MODE REGISTER
00DC      +1 159 PCA0CPM2    DATA 0DCH ; PCA MODULE 2 MODE REGISTER
00E0      +1 160 ACC         DATA 0E0H ; ACCUMULATOR
00E1      +1 161 XBR0       DATA 0E1H ; PORT I/O CROSSBAR CONTROL 0
00E2      +1 162 XBR1       DATA 0E2H ; PORT I/O CROSSBAR CONTROL 1
00E3      +1 163 OSCLCN     DATA 0E3H ; LOW-FREQUENCY OSCILLATOR CONTROL
00E4      +1 164 IT01CF     DATA 0E4H ; INT0/INT1 CONFIGURATION
00E6      +1 165 EIE1       DATA 0E6H ; EXTENDED INTERRUPT ENABLE 1
00E8      +1 166 ADC0CN     DATA 0E8H ; ADC0 CONTROL
00E9      +1 167 PCA0CPL1    DATA 0E9H ; PCA CAPTURE 1 LOW
00EA      +1 168 PCA0CPH1    DATA 0EAH ; PCA CAPTURE 1 HIGH
00EB      +1 169 PCA0CPL2    DATA 0EBH ; PCA CAPTURE 2 LOW
00EC      +1 170 PCA0CPH2    DATA 0ECH ; PCA CAPTURE 2 HIGH
00EF      +1 171 RSTSRC     DATA 0EFH ; RESET SOURCE CONFIGURATION/STATUS
00F0      +1 172 B          DATA 0F0H ; B REGISTER
00F1      +1 173 P0MDIN     DATA 0F1H ; PORT 0 INPUT MODE CONFIGURATION
00F2      +1 174 P1MDIN     DATA 0F2H ; PORT 1 INPUT MODE CONFIGURATION
00F6      +1 175 EIP1       DATA 0F6H ; EXTENDED INTERRUPT PRIORITY 1
00F8      +1 176 SPI0CN     DATA 0F8H ; SPI CONTROL
00F9      +1 177 PCA0L      DATA 0F9H ; PCA COUNTER LOW
00FA      +1 178 PCA0H      DATA 0FAH ; PCA COUNTER HIGH
00FB      +1 179 PCA0CPL0    DATA 0FBH ; PCA CAPTURE 0 LOW
00FC      +1 180 PCA0CPH0    DATA 0FCH ; PCA CAPTURE 0 HIGH
00FF      +1 181 VDM0CN     DATA 0FFH ; VDD MONITOR CONTROL
          +1 182 ;
          +1 183 ;
          +1 184 ;-----
          +1 185 ;BIT DEFINITIONS
          +1 186 ;
          +1 187 ; TCON 088H
008F      +1 188 TF1         BIT 08FH ; TIMER 1 OVERFLOW FLAG
008E      +1 189 TR1         BIT 08EH ; TIMER 1 ON/OFF CONTROL
008D      +1 190 TF0         BIT 08DH ; TIMER 0 OVERFLOW FLAG

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008C      +1 191 TR0          BIT 08CH      ; TIMER 0 ON/OFF CONTROL
008B      +1 192 IE1         BIT 08BH      ; EXT. INTERRUPT 1 EDGE FLAG
008A      +1 193 IT1         BIT 08AH      ; EXT. INTERRUPT 1 TYPE
0089      +1 194 IEO         BIT 089H      ; EXT. INTERRUPT 0 EDGE FLAG
0088      +1 195 ITO         BIT 088H      ; EXT. INTERRUPT 0 TYPE
          +1 196
          +1 197           ; SCON0 098H
009F      +1 198 SOMODE      BIT 09FH      ; UART 0 MODE
009D      +1 199 MCE0        BIT 09DH      ; UART 0 MCE
009C      +1 200 RENO         BIT 09CH      ; UART 0 RX ENABLE
009B      +1 201 TB80        BIT 09BH      ; UART 0 TX BIT 8
009A      +1 202 RB80        BIT 09AH      ; UART 0 RX BIT 8
0099      +1 203 TIO         BIT 099H      ; UART 0 TX INTERRUPT FLAG
0098      +1 204 RIO         BIT 098H      ; UART 0 RX INTERRUPT FLAG
          +1 205
          +1 206           ; IE 0A8H
00AF      +1 207 EA          BIT 0AFH      ; GLOBAL INTERRUPT ENABLE
00AE      +1 208 ESPIO       BIT 0AEH      ; SPI0 INTERRUPT ENABLE
00AD      +1 209 ET2         BIT 0ADH      ; TIMER 2 INTERRUPT ENABLE
00AC      +1 210 ES0         BIT 0ACH      ; UART0 INTERRUPT ENABLE
00AB      +1 211 ET1         BIT 0ABH      ; TIMER 1 INTERRUPT ENABLE
00AA      +1 212 EX1         BIT 0AAH      ; EXTERNAL INTERRUPT 1 ENABLE
00A9      +1 213 ET0         BIT 0A9H      ; TIMER 0 INTERRUPT ENABLE
00A8      +1 214 EX0         BIT 0A8H      ; EXTERNAL INTERRUPT 0 ENABLE
          +1 215
          +1 216           ; IP 0B8H
00BE      +1 217 PSPIO       BIT 0BEH      ; SPI0 PRIORITY
00BD      +1 218 PT2         BIT 0BDH      ; TIMER 2 PRIORITY
00BC      +1 219 PS0         BIT 0BCH      ; UART0 PRIORITY
00BB      +1 220 PT1         BIT 0BBH      ; TIMER 1 PRIORITY
00BA      +1 221 PX1         BIT 0BAH      ; EXTERNAL INTERRUPT 1 PRIORITY
00B9      +1 222 PT0         BIT 0B9H      ; TIMER 0 PRIORITY
00B8      +1 223 PX0         BIT 0B8H      ; EXTERNAL INTERRUPT 0 PRIORITY
          +1 224
          +1 225           ; SMB0CN 0C0H
00C7      +1 226 MASTER      BIT 0C7H      ; SMBUS 0 MASTER/SLAVE
00C6      +1 227 TXMODE      BIT 0C6H      ; SMBUS 0 TRANSMIT MODE
00C5      +1 228 STA         BIT 0C5H      ; SMBUS 0 START FLAG
00C4      +1 229 STO         BIT 0C4H      ; SMBUS 0 STOP FLAG
00C3      +1 230 ACKRQ       BIT 0C3H      ; SMBUS 0 ACKNOWLEDGE REQUEST
00C2      +1 231 ARBLOST     BIT 0C2H      ; SMBUS 0 ARBITRATION LOST
00C1      +1 232 ACK         BIT 0C1H      ; SMBUS 0 ACKNOWLEDGE FLAG
00C0      +1 233 SI          BIT 0C0H      ; SMBUS 0 INTERRUPT PENDING FLAG
          +1 234
          +1 235           ; TMR2CN 0C8H
00CF      +1 236 TF2H        BIT 0CFH      ; TIMER 2 HIGH BYTE OVERFLOW FLAG
00CE      +1 237 TF2L        BIT 0CEH      ; TIMER 2 LOW BYTE OVERFLOW FLAG
00CD      +1 238 TF2LEN      BIT 0CDH      ; TIMER 2 LOW BYTE INTERRUPT ENABLE
00CC      +1 239 TF2CEN      BIT 0CCH      ; TIMER 2 LFO CAPTURE ENABLE
00CB      +1 240 T2SPLIT     BIT 0CBH      ; TIMER 2 SPLIT MODE ENABLE
00CA      +1 241 TR2         BIT 0CAH      ; TIMER 2 ON/OFF CONTROL
00C8      +1 242 T2XCLK      BIT 0C8H      ; TIMER 2 EXTERNAL CLOCK SELECT
          +1 243
          +1 244           ; PSW 0D0H
00D7      +1 245 CY          BIT 0D7H      ; CARRY FLAG
00D6      +1 246 AC          BIT 0D6H      ; AUXILIARY CARRY FLAG
00D5      +1 247 F0          BIT 0D5H      ; USER FLAG 0
00D4      +1 248 RS1         BIT 0D4H      ; REGISTER BANK SELECT 1
00D3      +1 249 RS0         BIT 0D3H      ; REGISTER BANK SELECT 0
00D2      +1 250 OV          BIT 0D2H      ; OVERFLOW FLAG
00D1      +1 251 F1          BIT 0D1H      ; USER FLAG 1
00D0      +1 252 P           BIT 0D0H      ; ACCUMULATOR PARITY FLAG
          +1 253
          +1 254           ; PCA0CN 0D8H
00DF      +1 255 CF          BIT 0DFH      ; PCA 0 COUNTER OVERFLOW FLAG
00DE      +1 256 CR          BIT 0DEH      ; PCA 0 COUNTER RUN CONTROL BIT

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00DA      +1 257   CCF2          BIT 0DAH      ; PCA 0 MODULE 2 INTERRUPT FLAG
00D9      +1 258   CCF1          BIT 0D9H      ; PCA 0 MODULE 1 INTERRUPT FLAG
00D8      +1 259   CCF0          BIT 0D8H      ; PCA 0 MODULE 0 INTERRUPT FLAG
          +1 260           ; ADC 0 WINDOW INTERRUPT FLAG
          +1 261           ; ADC0CN 0E8H
00EF      +1 262   ADOEN          BIT 0EFH      ; ADC 0 ENABLE
00EE      +1 263   ADOEM          BIT 0EEH      ; ADC 0 TRACK MODE
00ED      +1 264   ADOINT         BIT 0EDH      ; ADC 0 EOC INTERRUPT FLAG
00EC      +1 265   ADOBUSY        BIT 0ECH      ; ADC 0 BUSY FLAG
00EB      +1 266   ADOWIN          BIT 0EBH      ; ADC 0 WINDOW INTERRUPT FLAG
00EA      +1 267   AD0CM2         BIT 0EAH      ; ADC 0 CONVERT START MODE BIT 2
00E9      +1 268   AD0CM1         BIT 0E9H      ; ADC 0 CONVERT START MODE BIT 1
00E8      +1 269   AD0CM0         BIT 0E8H      ; ADC 0 CONVERT START MODE BIT 0
          +1 270           ; SPI0CN 0F8H
          +1 271           ; SPI 0 INTERRUPT FLAG
00FF      +1 272   SPIF           BIT 0FFH      ; SPI 0 WRITE COLLISION FLAG
00FE      +1 273   WCOL           BIT 0FEH      ; SPI 0 MODE FAULT FLAG
00FD      +1 274   MODF           BIT 0FDH      ; SPI 0 RX OVERRUN FLAG
00FC      +1 275   RXOVRN         BIT 0FCH      ; SPI 0 SLAVE SELECT MODE 1
00FB      +1 276   NSSMD1         BIT 0FBH      ; SPI 0 SLAVE SELECT MODE 0
00FA      +1 277   NSSMD0         BIT 0FAH      ; SPI 0 TX BUFFER EMPTY FLAG
00F9      +1 278   TXBMT          BIT 0F9H      ; SPI 0 SPI ENABLE
00F8      +1 279   SPIEN          BIT 0F8H
          280
          281           ; tick constant:
          282
00E1      283   ITICK      EQU      225           ; osc = 3mhz and rfd data rate is 10kbs
          284
          285           ; 185 = 9600
          286           ; 221 = 19200
          287           ; 225 = 22600
          288           ; 230 = 27222
          289           ; memory address constants
          290
          291   ;AKMB      EQU      038H           ; ACK buffer start address (future)
0039      292   LNAK      EQU      039H           ; ACK length byte
003A      293   TPAK      EQU      03AH           ; ACK type byte
003B      294   TPAK      EQU      03BH           ; ACK TO/FROM byte
003C      295   IDAK      EQU      03CH           ; ACK packet ID byte
          296
0040      297   TXMB      EQU      040H           ; TX buffer start address (future)
0041      298   LNTX      EQU      041H           ; TX length byte
0042      299   TPTX      EQU      042H           ; TX type byte
0043      300   TFTX      EQU      043H           ; TX TO/FROM byte
0044      301   IDTX      EQU      044H           ; TX packet ID byte
0045      302   CMTX      EQU      045H           ; TX (host) command byte
          303
          304
0060      305   RXMB      EQU      060H           ; RX buffer start address (future)
0061      306   LNRX      EQU      061H           ; RX length byte
0062      307   TPRX      EQU      062H           ; RX type byte
0063      308   TFRX      EQU      063H           ; RX TO/FROM byte
0064      309   IDRX      EQU      064H           ; RX packet ID byte
0065      310   CMRX      EQU      065H           ; RX command byte
          311
          312
          313   ;*****
00F8      314   SPI0CN     EQU      0f8h           ; spio stat
00A1      315   SPI0CFG     EQU      0a1h           ; spio config
00A2      316   SPI0CKR     EQU      0a2h           ;
          317
          pio clock speed
00A3      317   SPI0DAT     EQU      0a3h           ; spi data read/write

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318 ;*****
319
320
321 ; type, framing and RangeTest constants
322
0000 323 RSVT EQU 000H ; reserved type
0010 324 ACKT EQU 010H ; RF ACK type
0020 325 MSGT EQU 020H ; RF message type
0040 326 HTCT EQU 040H ; host command type
0080 327 RXCT EQU 080H ; RF command type
328
0002 329 STX EQU 002H ; ASCII STX control character (future)
0006 330 TACK EQU 006H ; ASCII ACK control character
0015 331 TNAK EQU 015H ; ASCII NAK control character (future)
00C0 332 FEND EQU 0C0H ; FEND framing character
333
00E2 334 SOPL EQU 0E2H ; SOP low correlator pattern
00E2 335 SOPH EQU 0E2H ; SOP high correlator pattern
336
0002 337 RTTM EQU 002H ; 0.20 s RangeTest interval 14
338
339 ; frame check sequence (FCS) constants
340
00FF 341 FCSS EQU 0FFH ; FCS seed
0084 342 FCSH EQU 084H ; FCS high XOR mask
0008 343 FCSL EQU 008H ; FCS low XOR mask
00F0 344 FCVH EQU 0F0H ; FCS valid high byte pattern
00B8 345 FCVL EQU 0B8H ; FCS valid low byte pattern
346
347 ; stack: 08H - 015H (14 bytes)
348
349 ; bit labels (bytes 020H - 023H)
350
0000 351 DCRON EQU 000H ; RX data & clock recovery flag
0001 352 RXSMP EQU 001H ; RX input sample
0002 353 LRXSM EQU 002H ; last RX input sample
0003 354 RXBIT EQU 003H ; RX input bit
0004 355 SOPFLG EQU 004H ; SOP detect flag
0005 356 RXSFLG EQU 005H ; RX symbol flag
0006 357 FCSB EQU 006H ; FCS message bit
0007 358 OKFLG EQU 007H ; RX FCS OK flag
0008 359 SIHLD EQU 008H ; RX enable host flag
0009 360 NHFLG EQU 009H ; no RX header flag
000A 361 SNFLG EQU 00AH ; send NAK to host flag
362
000B 363 RAFLG EQU 00BH ; RF ACK type flag
000C 364 RMFLG EQU 00CH ; RF message type flag
000D 365 RCFLG EQU 00DH ; RF command type flag
366
000E 367 SIFLG EQU 00EH ; TX enable host flag
000F 368 TOFLG EQU 00FH ; host timeout flag
369
0010 370 HTFLG EQU 010H ; host traffic type flag
0011 371 HCFLG EQU 011H ; host command type flag
372
0012 373 TXFLG EQU 012H ; TX active flag
0013 374 TMFLG EQU 013H ; TX message flag
0014 375 TSFLG EQU 014H ; output TX sample flag
0015 376 TXBIT EQU 015H ; TX message bit
377
0016 378 RTFLG EQU 016H ; RangeTest active flag
0017 379 RSFLG EQU 017H ; RangeTest message flag
380
0018 381 PIFLG EQU 018H ; ping active flag
0019 382 PMFLG EQU 019H ; ping message flag
383

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001A      384      THFLG      EQU      01AH      ; TO here flag
001B      385      RHFLG      EQU      01BH      ; Repeat here flag
          386
001C      387      FLG1       EQU      01CH      ; spare flag 1
001D      388      FLG2       EQU      01DH      ; spare flag 2
001E      389      RTFLG1     EQU      01EH      ; spare flag 3
001F      390      RSFLG2     EQU      01FH      ; spare flag 4
          391
          392      ; register usage
          393
          394      ; R0          RX data pointer
          395      ; R1          TX data pointer
          396      ; R2          data & clock recovery (DCR)
          397      ; R3          RX FCS buffer A
          398      ; R4          not used
          399      ; R5          TX FCS buffer A
          400      ; R6          TX FCS buffer B
          401      ; R7          RX FCS buffer B
          402
          403      ; byte labels
          404
0016      405      RXBL       EQU      016H      ; RX low buffer, SOP correlator, etc.
0017      406      RXBH       EQU      017H      ; RX high buffer, SOP correlator, etc.
0018      407      RXBB       EQU      018H      ; RX symbol decode byte buffer
0019      408      RMBYC      EQU      019H      ; RX message byte counter (LNRX 1st byte)
001A      409      RMFCS      EQU      01AH      ; RX FCS byte buffer
001B      410      RMSBC      EQU      01BH      ; RX symbol bit counter
001C      411      RMFCC      EQU      01CH      ; RX message FCS counter, etc.
          412
001D      413      TXSI       EQU      01DH      ; TX start symbol index
001E      414      TMFCC      EQU      01EH      ; TX timer & loop counter
001F      415      TXSMC      EQU      01FH      ; TX output sample counter
0024      416      TMBIC      EQU      024H      ; TX message bit counter
0025      417      TMBYT      EQU      025H      ; TX message byte buffer
0026      418      TMBYC      EQU      026H      ; TX message byte counter (including FENDs)
0027      419      TXSL       EQU      027H      ; TX message symbol low buffer
0028      420      TXSH       EQU      028H      ; TX message symbol high buffer
0029      421      TMFCS      EQU      029H      ; TX FCS byte buffer
002A      422      TXTL       EQU      02AH      ; TX timer low byte
002B      423      TXTH       EQU      02BH      ; TX timer high byte
002C      424      TXCNT      EQU      02CH      ; TX retry counter
002D      425      IDBUF      EQU      02DH      ; Packet ID buffer
002E      426      TFBUF      EQU      02EH      ; TO/FROM address buffer
002F      427      TEMPB      EQU      02FH      ; Temp buffer
          428
0030      429      RTID       EQU      030H      ; RangeTest ID buffer
0031      430      RTTH       EQU      031H      ; RangeTest timer high byte
          431
0032      432      BUF01      EQU      032H      ; spare buffer 1
0033      433      BUF02      EQU      033H      ; spare buffer 2
0034      434      BUF03      EQU      034H      ; spare buffer 3
0035      435      BUF04      EQU      035H      ; spare buffer 4
0036      436      BUF05      EQU      036H      ; spare buffer 5
0037      437      BUF06      EQU      037H      ; spare buffer 6
0038      438      fhss       EQU      038h      ;
003D      439      fhcnt      EQU      03dh      ; searching counter if lost
          440
          441      ; I/O pins for SDIO demo
          442
0091      443      CL1        EQU      P1.1      ; ASH Radio CNTRL1 *** 0 = TX, 1 = RX
0090      444      CL0        EQU      P1.0      ; ASH Radio CNTRL0 *** 1 = TX, 1 = RX
          445
          446      ;The Same for Analog mode
0094      447      RXPIN       EQU      P1.4      ; RX input pin (non-inverted)
0093      448      TXPIN       EQU      P1.3      ; TX output pin (on = 1) Was 3
          449

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```

450
0082 451 PCRCV EQU P0.2 ; LED (on = 1) 5
0082 452 RFRCV EQU P0.2 ; LED (on = 1) Was 1.6
0083 453 RXI EQU P0.3 ; LED (on = 1) Was 7,3
454
0097 455 ID0 EQU P1.7
; Range Test Jumper
456

457
0083 458 Closed EQU P0.3 ; LED White
0081 459 Opening EQU P0.1 ; LED Amber
0082 460 Open EQU P0.2 ; LED yellow
0080 461 Closing EQU P0.0 ; LED RED
462
463
464 ; start of code
465
0000 466 ORG 00H ; hardware reset
0000 01FF 467 reset: AJMP start ; jump to start
468
000B 469 ORG 0BH ; timer 0 interrupt vector
470
471 ; timer 0 interrupt service routine, 3 ticks/RF bit period
472
000B C0D0 473 tick: PUSH PSW ; push status
000D C0E0 474 PUSH ACC ; push accumulator
000F 30006D 475 JNB DCRON,tic0 ; skip if DCR idle
476
477 ; RX data & clock recovery
478
0012 A201 479 dcr: MOV C,RXSMP ; store RX sample
0014 9202 480 MOV LRXSM,C ; as last RX sample
0016 A294 481 MOV C,RXPIN ; read RX input pin (non-inverted)
0018 9201 482 MOV RXSMP,C ; and store new RX sample
001A 300201 483 dcr0: JNB LRXSM,dcr1 ; if last sample 1
001D B3 484 CPL C ; complement new sample
001E 5004 485 dcr1: JNC dcr2 ; if no edge jump to dcr2
0020 7A00 486 MOV R2,#0 ; else clear R2
0022 017C 487 AJMP dcr_d ; dcr done this tick
0024 0A 488 dcr2: INC R2 ; else increment R2
0025 BA0106 489 CJNE R2,#1,dcr3 ; if not 1 jump to dcr3
0028 A201 490 MOV C,RXSMP ; else load RXSMP
002A 9203 491 MOV RXBIT,C ; into RXBIT
002C 0135 492 AJMP dcr4 ; jump to dcr4
002E BA034B 493 dcr3: CJNE R2,#3,dcr_d ; if not 3 jump dcr_d
0031 7A00 494 MOV R2,#0 ; else clear R2
0033 017C 495 AJMP dcr_d ; done this tick
0035 20042B 496 dcr4: JB SOPFLG,dcr6 ; skip after SOP detect
497
498 ; detect start-of packet-symbol (set SOP flag)
499
0038 E516 500 MOV A,RXBL ; else get RXBL
003A C3 501 CLR C ; clear carry
003B 33 502 RLC A ; rotate left through carry
003C 300302 503 JNB RXBIT,dcr5 ; if bit 0 jump to dcr5
003F D2E0 504 SETB ACC.0 ; else set lsb
0041 F516 505 dcr5: MOV RXBL,A ; store RXBL
0043 E517 506 MOV A,RXBH ; get RXBH
0045 33 507 RLC A ; shift and pull in carry
0046 F517 508 MOV RXBH,A ; store RXBH
0048 B4E231 509 CJNE A,#SOPH,dcr_d ; done if not SOPH
004B E516 510 MOV A,RXBL ; else get low buffer
004D B4E22C 511 CJNE A,#SOPL,dcr_d ; done if not SOPL
0050 751600 512 MOV RXBL,#0 ; clear RX low buffer
0053 751B06 513 MOV RMSBC,#6 ; set counter, 6 bits/half-symbol

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```

0056 90078B      514      MOV      DPTR,#rx_smb1 ; point to RX symbol table
0059 C205        515      CLR      RXSFLG        ; clear RX symbol flag
005B C208        516      CLR      SIHLD        ; hold off host serial port
005D D204        517      SETB    SOPFLG        ; set SOP detected flag
005F D283        518      setb    RXI          ; turn RXI LED on
0061 017C        519      AJMP    dcr_d        ; done for now
520
521
522      ; compile 6-bit half-symbols, synchronize rxmsg subroutine with RXSFLG flag
523
0063 E516        524      dcr6:   MOV      A,RXBL        ; get RXBL
0065 C3          525      CLR      C            ; clear carry
0066 33          526      RLC      A            ; shift left
0067 300302      527      JNB     RXBIT,dcr7     ; if 0 bit jump to dcr7
006A D2E0        528      SETB    ACC.0        ; else set lsb
006C F516        529      dcr7:   MOV      RXBL,A      ; store RXBL
006E D51B0B      530      DJNZ    RMSBC,dcr_d   ; if not 0 jump to dcr_d
0071 851618      531      MOV     RXBB,RXBL     ; get symbol
0074 751600      532      MOV     RXBL,#0      ; clear RXBL
0077 751B06      533      MOV     RMSBC,#6     ; reset counter
007A D205        534      SETB    RXSFLG       ; set symbol flag for rxmsg
007C 20044B      535      dcr_d:  JB      SOPFLG,tick_d ; skip if SOP detected
536
537      ; output TX bit samples (TXSMC = 0 synchronizes txmsg subroutine)
538
007F 30140A      539      tic0:   JNB     TSFLG,tic1 ; skip if TX sample out idle
0082 E51F        540      MOV     A,TXSMC     ; else get sample count
0084 6006        541      JZ      tic1        ; skip if 0
0086 A215        542      MOV     C,TXBIT     ; else load TX bit
0088 9293        543      MOV     TXPIN,C     ; into TX output pin
008A 151F        544      DEC     TXSMC       ; decrement sample count
545
546      ; timeout on serial character stream from host (clear hang-ups)
547
008C 300F0C      548      tic1:   JNB     TOFLG,tic2 ; skip if host message timeout idle
008F 051E        549      INC     TMFCC       ; else bump timeout counter
0091 E51E        550      MOV     A,TMFCC     ; get counter
0093 B49605      551      CJNE   A,#150,tic2 ; skip if counter not 150
0096 C20F        552      CLR     TOFLG       ; else reset timeout flag
0098 751E00      553      MOV     TMFCC,#0    ; reset counter
554
555      ; event timers
556
009B 052A        557      tic2:   INC     TXTL        ; bump TX timer low
009D E52A        558      MOV     A,TXTL     ; load TX timer low
009F 7029        559      JNZ    tick_d      ; done if no rollover (8.89 ms cycle)
560
561      ; RangeTest event
562      tic2_c:
563      ;      MOV     C,ID0        ; read ID0
564      ;      JC      tic3        ; skip if no ID0 jumper
00A1 20140B      565      JB     TSFLG,tic3 ; skip if TX busy
00A4 301608      566      JNB    RTFLG,tic3 ; skip if RangeTest idle
00A7 D53105      567      DJNZ   RTHH,tic3 ; decrement RTHH, jump if not 0
00AA D217        568      SETB   RSFLG       ; else set RangeTest message flag,
00AC 753102      569      MOV     RTHH,#RTTM ; reload RTHH high
570
571      ; TX retry event
572
00AF 301218      573      tic3:   JNB     TXFLG,tick_d ; skip if send TX packet idle
00B2 D52B15      574      DJNZ   TXTH,tick_d ; decrement TXTH, done if not 0
00B5 D213        575      SETB   TMFLG       ; else set TM message flag
576
577      ; load semi-random TX retry interval
578
00B7 9007CB      579      MOV     DPTR,#delay ; point to delay table

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```

00BA E58B      580          MOV     A,TL1      ; get random table offset
00BC 5407      581          ANL     A,#07H     ; mask out upper 5 bits
00BE 93        582          MOVC    A,@A+DPTR  ; load byte from table
00BF F52B      583          MOV     TXTH,A     ; into TX delay high
584
585          ; shut down TX and NAK host after 8 tries
586
00C1 E52C      587          MOV     A,TXCNT    ; load retry count
00C3 B40904    588          CJNE   A,#9,tick_d ; if not 9 jump to tick_d
00C6 C213      589          CLR     TMFLG     ; else reset send TX message
00C8 D20A      590          SETB   SNFLG     ; set send TX NAK flag
591
592          ; restore and return from isr
593
00CA D5361B    594          tick_d: DJNZ   BUF05,tick_d1 ; Hart beat delay counter 1
00CD D53718    595          counter      DJNZ   BUF06,tick_d1 ; hart beat delay
                    2
00D0 20800D    596          JB     Closing,tick_d2 ; flash the led, if set clr it
00D3 7404      597          MOV     A,#4     ; on short period of time
00D5 F537      598          MOV     BUF06,A   ; 1
                    oad counter
00D7 D280      599          SETB   Closing ; led on
600
00D9 30160C    601          JNB    RTFLG,tick_d1 ; skip if RangeTest idle
00DC C204      602          CLR     SOPFLG
603
00DE 01E8      604          tick_d2: AJMP   tick_d1
00E0 C280      605          CLR     Closing ; led off
00E2 C283      606          CLR     Closed
00E4 7480      607          MOV     A,#128   ; off longer than on
00E6 F537      608          MOV     BUF06,A   ; 1
                    oad counter
00E8 200500    609          tick_d1: JB     RXSFLG,tick_d3 ; prevent lock ups on symbol detect
610
00EB          611          tick_d3:
00EB D0E0      612          POP     ACC      ; pop accumulator
00ED D0D0      613          POP     PSW     ; pop status
00EF 32        614          RETI          ; interrupt done
615
616          ;***** RX fhss CHANNEL CHANGE *****
00F0 75A3A1    617          chan:  mov     SPIODAT,#0alh ; Sent MSB of freq
00F3 F10F      618          ACALL  spio_wait ; WAIT FOR SPI
619          ;          mov     fhss,CMRX ; get current channel
00F5 0538      620          inc     fhss     ; bump it
00F7 E538      621          MOV     A,fhss   ; fh offset count
00F9 B41901    622          cjne   a,#25,h4a ; 25 channels max now
00FC E4        623          clr     a         ; da
00FD F538      624          h4a:  MOV     fhss,a   ; save channel
00FF AC38      625          mov     R4,fhss   ; make loop count
0101 E4        626          CLR     A         ; clear acc to make channe
                    1
0102 0C        627          inc     r4
                    ; inc loop count
0103 240A      628          h2a:  add     a,#10     ; channel 10* R4
0105 DCFC      629          djnz   r4,h2a    ; loop count
0107 F5A3      630          mov     SPIODAT,A ; Send LSB of Freq
0109 22        631          ret
632          ;          ACALL  spio_wait ; wait for spi to finish
633          ;          ACALL  wait    ; ~20us to change
channels
634          ;          ACALL  wait
635          ;*****
636
637          ;***** restart FHSS Channel *****
010A          638          chan0:
010A 75A3A1    639          mov     SPIODAT,#0alh ;a
                    ; Sent MSB of freq

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010D F10F      640                                ACALL    spio_wait
010F 7C01      641                                mov     R4,#1
0111 E4        642                                CLR     A
0112 0C        643                                inc     r4
0113 240A      644      h3z:      add     a,#10
0115 DCFC      645                                djnz   r4,h3z
0117 F5A3      646                                mov     SPIODAT,A ;#063h ; Send LSB of Freq
0119 F10F      647      ACALL    spio_wait
011B 716E      648      ACALL    wait
011D 22        649      ret
011E          650      ;*****
011F          651
0120          652
00FF          653      start:   ORG     0FFH      ; above interrupt code space
00FF D101      654      ACALL    setup      ; initialization code
0101 753D08    655
0102          656      mov     fhcnt,#8    ; 16 tries
0103          657
0104          658
0104 D283      659      SETB    Closed      ; Flash the leds
0106 715F      660      ACALL    led
0108 D281      661                                SETB    Opening      ; led lamp test delay
010A 715F      662      ACALL    led
010C D282      663                                SETB    Open         ; led lamp test delay
010E 715F      664      ACALL    led
0110 D280      665                                SETB    Closing      ; led lamp test delay
0112 715F      666      ACALL    led
0114 715F      667      ACALL    led
0116 715F      668      ACALL    led
0118 715F      669      ACALL    led
011A 715F      670      ACALL    led
011C C283      671      CLR     Closed
011E 715F      672      ACALL    led
0120 C281      673                                CLR     Opening      ; led lamp test delay
0122 715F      674      ACALL    led
0124 C282      675                                CLR     Open         ; led lamp test delay
0126 715F      676      ACALL    led
0128 C280      677                                CLR     Closing      ; led lamp test delay
0129          678
012A D19E      679      ACALL    rfic
012B          680
012C 715F      681      ACALL    led
012E 715F      682      ACALL    led
0130 715F      683      ACALL    led
0131          684
0132 F104      685      ACALL    tx_off
0133          686
0134 715F      687      ACALL    led
0136 715F      688      ACALL    led
0138 715F      689      ACALL    led
0139          690
013A 75A3A1    691      mov     SPIODAT,#0a1h ;a
013B          692      ; Sent MSB of freq
013D F10F      692      ACALL    spio_wait
013F 7C01      693      mov     R4,#1
0141 E4        694      CLR     A
0142 0C        695      inc     r4
0143 240A      696      h3z:      add     a,#10
0145 DCFC      697                                djnz   r4,h3
0147 F5A3      698      mov     SPIODAT,A ;#063h ; Send LSB of Freq
0149 F10F      699      ACALL    spio_wait
014B 716E      700      ACALL    wait
014C          701

```

```

702
703
704 ; main program loop
705
014D main:
706
707
708
709
014D 301704 710 JNB RSFLG,mn0 ; skip if RangeTest not queued
0150 71D0 711 ACALL do_ra ; else do RangeTest
0152 216E 712 AJMP mn3 ; jump to RX SOP detect
0154 30980B 713 mn0: JNB RI0,mn1 ; skip if RI clear
0157 300808 714 JNB SIHLD,mn1 ; skip if serial in idled by RX
015A 300E05 715 JNB SIFLG,mn1 ; skip if serial in idled by TX
015D 201802 716 JB PIFLG,mn1 ; skip if ping active
0160 71EA 717 ACALL do_ht ; else service host
0162 301302 718 mn1: JNB TMFLG,mn2 ; skip if transmit not queued
0165 9124 719 ACALL do_rt ; else do transmit retry
0167 300A04 720 mn2: JNB SNFLG,mn3 ; skip if send NAK flag clear
016A 711C 721 ACALL aksnd ; else send NAK to host
016C B1A9 722 ACALL txmrs ; and master rest TX
016E 3004DC 723 mn3: JNB SOPFLG,main ; if not SOP loop to main
0171 2016D9 724 JB RTFLG,main
0174 317D 725 ACALL do_rx ; else do RX message
0176 3019D4 726 mn4: JNB PMFLG,main ; if ping idle loop to main
0179 910F 727 ACALL do_pi ; else do ping
017B 214D 728 mn_d: AJMP main ; loop to main
729
730 ; receive message, transmit ACK, do command or send message to host
731
017D 31E0 732 do_rx: ACALL rxmsg ; receive packet
017F C200 733 CLR DCRON ; idle RX DCR
0181 511A 734 ACALL rxfcs ; test packet FCS
0183 30074C 735 JNB OKFLG,rx4 ; jump to reset RX if error
0186 201649 736 JB RTFLG,rx4 ; jump if RangeTest active
0189 5128 737 ACALL rxto ; test packet TO address
018B 301A44 738 JNB THFLG,rx4 ; jump to reset if not TO here
018E 5141 739 ACALL rxtyp ; else get RX packet type
0190 300B09 740 JNB RAFLG,rx1 ; skip if not an RX ACK
0193 201802 741 JB PIFLG,rx0 ; skip if RX ACK for ping
0196 711C 742 ACALL aksnd ; else ACK host
0198 B1A9 743 rx0: ACALL txmrs ; master reset TX
019A 21D2 744 AJMP rx4 ; jump to reset RX
019C 745 rx1: ;**** add FH data to here ****
746 ; ACALL ackrx ; transmit ACK to sender
747
748
749 ;***** RX fhss CHANNEL CHANGE *****
019C 75A3A1 750 mov SPIODAT,#0a1h ; Sent MSB of freq

019F F10F 751 ACALL spio_wait ; WAIT FOR SPI
01A1 856538 752 mov fhss,CMRX ; get current channel
01A4 0538 753 inc fhss ; bump it
01A6 E538 754 MOV A,fhss ; fh offset count
01A8 B41801 755 cjne a,#24,h4 ; 25 channels max now
01AB E4 756 clr a ; da
01AC F538 757 h4: MOV fhss,a ; save channel
01AE AC38 758 mov R4,fhss ; make loop count
01B0 E4 759 CLR A ; clear acc to make channe

1
01B1 0C 760 inc r4
; inc loop count
01B2 240A 761 h2: add a,#10 ; channel 10* R4
01B4 DCFC 762 djnz r4,h2 ; loop count
01B6 F5A3 763 mov SPIODAT,A ; Send LSB of Freq
01B8 F10F 764 ACALL spio_wait ; wait for spi to finish

```

```

765 ;*****
766
767 ;          ACALL    ackrx          ; transmit ACK to sender
768
01BA 300D04      769          JNB      RCFLG,rx2      ; skip if not an RX command
01BD 51A5        770          ACALL    rxcmd          ; else do command
01BF 21D2        771          AJMP     rx4            ; and jump to reset RX
01C1 301809      772 rx2:      JNB      PIFLG,rx3      ; skip if ping disabled
01C4 201206      773          JB       TXFLG,rx3      ; skip if TXFLG set
01C7 51B6        774          ACALL    ld_tx           ; else load TX from RX, idle SIFLG
01C9 51DB        775          ACALL    ad_tx           ; address TX, set PMFLG
01CB 21D2        776          AJMP     rx4            ; jump to reset RX
01CD 300C02      777 rx3:      JNB      RMFLG,rx4      ; skip if not RX message
01D0 51EC        778          ACALL    htsnd          ; else send RX message to host
01D2 301602      779 rx4:      JNB      RTFLG,rx5      ; skip if RangeTest idle
01D5 715F        780          ACALL    led             ; else delay to light LED
01D7 717D        781 rx5:      ACALL    rxrst          ; reset RX, set SIHLD
01D9 D200        782          SETB     DCRON            ; enable RX DCR
01DB C299        783          CLR      T10             ; clear T10 flag
01DD C298        784          CLR      RI0            ; clear RI flag
01DF 22          785 rx_d:     RET              ; RX done
786
787 ; receive and de-symbolize message
788
01E0 3005FD      789 rxmsg:    JNB      RXSFLG,rxmsg    ; wait for RX symbol flag from isr
01E3 C205        790          CLR      RXSFLG          ; clear RX symbol flag
01E5 E518        791          MOV     A,RXBH          ; index into symbol table
01E7 93          792          MOVC   A,@A+DPTR        ; get table entry
01E8 C4          793          SWAP   A                ; swap to high nibble
01E9 F517        794          MOV     RXBH,A            ; into RXBH
01EB 3005FD      795 rxm2:     JNB      RXSFLG,rxm2      ; wait for symbol flag from isr
01EE C205        796          CLR      RXSFLG          ; clear flag
01F0 E518        797          MOV     A,RXBH          ; index into symbol table
01F2 93          798          MOVC   A,@A+DPTR        ; get table entry
01F3 4517        799          ORL    A,RXBH            ; add RXBH low
01F5 F517        800          MOV     RXBH,A            ; store in RXBH
01F7 A617        801          MOV     @R0,RXBH          ; and store in RX message buffer
01F9 B86115      802          CJNE   R0,#LNRX,rxm4      ; skip if not length byte
01FC E517        803          MOV     A,RXBH            ; else get first byte
01FE 543F        804          ANL    A,#63             ; mask upper 2 bits
0200 6009        805          JZ      rxm3              ; 0 is an error
0202 F519        806          MOV     RMBYC,A           ; load message byte counter
0204 F51C        807          MOV     RMFCC,A           ; and RX message loop counter
0206 C3          808          CLR    C                 ; clear borrow
0207 941F        809          SUBB   A,#31              ; compare number of bytes to 31
0209 4006        810          JC      rxm4              ; skip if < 31
020B 751904      811 rxm3:     MOV     RMBYC,#4           ; else force byte counter to 4 (force error)
020E 751C04      812          MOV     RMFCC,#4          ; and force loop counter to 4
0211 08          813 rxm4:     INC     R0                 ; bump pointer
0212 D51CCB      814          DJNZ   RMFCC,rxmsg        ; if not 0 get another byte
0215 7861        815          MOV     R0,#LNRX          ; reset RX message pointer
0217 C283        816          clr    RXI                ; turn LED off
0219 22          817 rxm_d:    RET              ; RX message done
818
819 ; build and test FCS
820
021A 85191C      821 rxfcs:    MOV     RMFCC,RMBYC      ; move byte count to loop counter
021D 861A        822 rxf0:     MOV     RMFCS,@R0          ; get next message byte
021F 08          823          INC     R0                 ; bump pointer
0220 719B        824          ACALL   b_rfcs            ; build FCS
0222 D51CF8      825          DJNZ   RMFCC,rxf0         ; loop for next byte
0225 71BF        826          ACALL   a_rfcs            ; test FCS
0227 22          827 rxf_d:    RET              ; RX FCS done
828
829 ; determine if packet is to here, and if so is it single or multi-hop
830

```

```

0228 E52E      831  rxto:   MOV     A,TFBUF      ; get local TO/FROM address
022A 540F      832        ANL     A,#15       ; mask to get local FROM address
022C F5F0      833        MOV     B,A         ; store FROM address
022E E563      834        MOV     A,TFRX      ; get T/F address from RX buffer
0230 C4        835        SWAP   A           ; swap - FROM/TO
0231 540F      836        ANL     A,#15       ; mask to get TO address
0233 B5F00A    837        CJNE   A,B,rxto_d  ; done if not TO here
0236 D21A      838        SETB   THFLG      ; else set TO here flag
0238 E562      839        MOV     A,TPRX     ; get RX type byte
023A 540F      840        ANL     A,#15       ; mask out upper nibble, get hops
023C 6002      841        JZ     rxto_d     ; done if single hop
023E D21B      842        SETB   RHFLG      ; else set repeat here flag
0240 22        843  rxto_d:  RET          ; done
          844
          845  ; determine RF packet type
          846
0241 E562      847  rxtyp:   MOV     A,TPRX     ; get RX type byte
0243 54F0      848        ANL     A,#240     ; mask out lower nibble, get type
0245 B42004    849        CJNE   A,#MSGT,rxto0 ; skip if not message
0248 D20C      850        SETB   RMFLG      ; else set RX message flag
024A 4160      851        AJMP   rxt_d     ; done
024C B48004    852  rxto0:   CJNE   A,#RXCT,rxto1 ; skip if not RX command
024F D20D      853        SETB   RCFLG      ; else set RX command flag
0251 4160      854        AJMP   rxt_d     ; done
0253 B4100A    855  rxto1:   CJNE   A,#ACKT,rxto_d ; done if not RX ACK
0256 E52E      856        MOV     A,TFBUF     ; else get local TO/FROM
0258 C4        857        SWAP   A           ; swap for FROM/TO
0259 B56304    858        CJNE   A,TFRX,rxto_d ; done if not RX TO/FROM
025C E52D      859        MOV     A,IDBUF     ; else get TX packet ID
          860  ; CJNE   A,IDRX,rxto_d ; done if not TX ID
025E D20B      861        SETB   RAFLG      ; else set RX ACK flag
0260 22        862  rxt_d:   RET          ; done
          863
          864  ; transmit ACK back to sending node
          865
0261 D282      866  ackrx:   SETB   Open
0263 7939      867        MOV     R1,#LNAK    ; load ACK pointer
0265 7706      868        MOV     @R1,#6     ; ACK length is 6 bytes
0267 752906    869        MOV     TMFCS,#6   ; load TX message FCS byte
026A B1D1      870        ACALL  b_tfcs     ; and build FCS
026C 09        871        INC     R1         ; bump pointer
026D 7710      872        MOV     @R1,#ACKT  ; store ACK type byte
026F 752910    873        MOV     TMFCS,#ACKT ; load TX message FCS byte
0272 B1D1      874        ACALL  b_tfcs     ; and build FCS
0274 09        875        INC     R1         ; bump pointer
0275 E563      876        MOV     A,TFRX     ; get TO/FROM byte
0277 C4        877        SWAP   A           ; swap TO/FROM addresses
0278 F7        878        MOV     @R1,A       ; add to ACK buffer
0279 F529      879        MOV     TMFCS,A       ; load TX message FCS byte
027B B1D1      880        ACALL  b_tfcs     ; and build FCS
027D 09        881        INC     R1         ; bump pointer
027E E564      882        MOV     A,IDRX     ; get packet ID byte
0280 F7        883        MOV     @R1,A       ; add ID to ACK message
0281 F529      884        MOV     TMFCS,A       ; load TX message FCS byte
0283 B1D1      885        ACALL  b_tfcs     ; and build FCS
0285 09        886        INC     R1         ; bump pointer
0286 B1F5      887        ACALL  a_tfcs     ; add FCS
0288 7939      888        MOV     R1,#LNAK    ; reset ACK pointer
028A 85262F    889        MOV     TEMPB,TMBC  ; store TX message TMBC
028D 752606    890        MOV     TMBC,#6     ; 6 bytes in ACK
0290 B129      891        ACALL  txmsg     ; send TX message
0292 E4        892        CLR     A           ; reset for next TX
0293 F525      893        MOV     TMBYT,A      ; clear TX message byte
0295 F51F      894        MOV     TXSMC,A     ; clear TX out count
0297 F527      895        MOV     TXSL,A     ; clear TX symbol low
0299 F528      896        MOV     TXSH,A     ; clear TX symbol high

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029B 7941      897      MOV      R1,#LNTX      ; point R1 to message start
029D 852F26    898      MOV      TMBYC,TEMPB  ; restore TX message TMBYC
02A0 C282      899      arx0:   clr      RFRCV      ; turn FCS LED off
02A2 C282      900      CLR      Open        ;
02A4 22        901      arx_d:   RET          ; RX ACK done
02A5 E565      902
02A7 B44204    903      ; do RX command (bounce on/off), reset RCFLG
02AA D218      904
02AC 41B3      905      rxcmd:   MOV      A,CMRX      ; get RX command
02AE B44E02    906      CJNE     A,#66,rxc0   ; skip if not bounce on
02B1 C218      907      SETB    PIFLG      ; else set RX message flag
02B3 C20D      908      AJMP    rxc1       ; done
02B5 22        909      rxc0:   CJNE     A,#78,rxc1 ; skip if not bounce off
02B6 C282      910      CLR      PIFLG      ; disable ping
02B8 1519      911      rxc1:   CLR      RCFLG     ; reset RX command flag
02BA 851926    912      rxc_d:   RET          ;
02BC 7861      913
02BD 7861      914      ; load TX buffer from RX buffer, idle SIFLG to block host input
02BF 7941      915
02C1 77C0      916      ld_tx:   CLR      PCRCV     ; turn PC LED on
02C3 08        917      DEC      RMBYC      ; adjust number of bytes to copy
02C4 09        918      MOV      TMBYC,RMBYC ; transfer RX count to TX count
02C5 1519      919      MOV      R0,#LNRX   ; reset RX buffer pointer
02C7 E6        920      MOV      R1,#LNTX   ; reset TX buffer pointer
02C8 F7        921      MOV      @R1,#FEND   ; load first FEND
02CA 09        922      INC      R0          ; bump RX pointer past FEND
02CB D519F9    923      INC      R1          ; bump TX pointer past FEND
02CE 77C0      924      DEC      RMBYC      ; decrement byte count
02D0 7861      925      ld0:    MOV      A,@R0      ; get RX byte
02D2 7941      926      MOV      @R1,A       ; load TX buffer
02D4 C20E      927      INC      R0          ; bump RX pointer
02D6 C282      928      INC      R1          ; bump TX pointer
02D8 D282      929      DJNZ    RMBYC,ld0   ; loop to load message
02DA 22        930      MOV      @R1,#FEND   ; add 2nd FEND
02DB E563      931      MOV      R0,#LNRX   ; reset RX buffer pointer
02DD C4        932      MOV      R1,#LNTX   ; reset TX buffer pointer
02DE F543      933      CLR      SIFLG      ; TX loaded, idle host
02E0 856444    934      ld1:   clr      RFRCV     ; turn FCS LED off
02E3 85432E    935      SETB    PCRCV      ; turn PC LED off
02E6 85442D    936      ld_d:   RET          ; load TX buffer done
02E9 D219      937
02EB 22        938      ld_d:   RET          ;
02EC C282      939      ; set TX TO/FROM address, ID, set PMFLG (ping message)
02ED 7941      940      ad_tx:   MOV      A,TFRX     ; get RX TO/FROM
02EE 1519      941      SWAP    A           ; swap TO/FROM
02EF 1519      942      MOV      TFTX,A      ; load TX TO/FROM
02F0 1519      943      MOV      IDTX,IDRX   ; load TX ID from RX ID
02F2 7861      944      MOV      TFBUF,TFTX  ; update local TO/FROM buffer
02F4 76C0      945      MOV      IDBUF,IDTX  ; update local ID buffer
02F6 08        946      SETB    PMFLG      ; enable ping message
02F8 1519      947      ad_d:   RET          ; TX address done
02FA 1519      948
02FB 1519      949      ; send received message to host with FEND framing
02FD 1519      950
02FE 1519      951      htsnd:   CLR      PCRCV     ; turn PC LED on
02FF 1519      952      DEC      RMBYC      ; don't send the
0300 1519      953      DEC      RMBYC      ; 2 FCS bytes
0301 1519      954      MOV      R0,#LNRX   ; reset RX message pointer
0302 1519      955      MOV      @R0,#FEND   ; replace number of bytes with FEND
0303 1519      956      ;      JNB      NHFLG,hts0 ; skip if no FEND/header flag reset
0304 1519      957      INC      R0          ; bump past FEND
0305 1519      958      DEC      RMBYC      ; decrement byte count
0306 1519      959      INC      R0          ; bump past FEND
0307 1519      960      DEC      RMBYC      ; decrement byte count
0308 1519      961      INC      R0          ; bump past Type
0309 1519      962      DEC      RMBYC      ; decrement byte count

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02FF 08          963          INC      R0          ; bump past TO/FROM
0300 1519        964          DEC      RMBYC       ; decrement byte count
0302 08          965          INC      R0          ; bump past ID
0303 1519        966          DEC      RMBYC       ; decrement byte count
0305 C299        967          hts0:   CLR      TI0       ; clear TI0 flag
0307 8699        968          hts1:   MOV      SBUF0,@R0 ; send byte
0309 3099FD      969          hts2:   JNB     TI0,hts2 ; wait until byte sent
030C C299        970          CLR      TI0       ; clear TI0 flag
030E 08          971          INC      R0          ; bump pointer
030F D519F5      972          DJNZ    RMBYC,hts1 ; loop to send message
0312 200902      973          ;       JB      NHFLG,hts4 ; skip if no FEND/header flag set
          974          ;       MOV     SBUF0,#FEND ; add 2nd FEND
          975          ;hts3:  JNB     TI0,hts3 ; wait until byte sent
0315 C299        976          CLR      TI0       ; clear TI0 flag
0317 C282        977          hts4:   clr     RFRCV   ; turn FCS LED off
0319 D282        978          SETB    PCRCV      ; turn PC LED off
031B 22          979          hts_d:  RET          ; send RX message done
          980
          981          ; send ACK/NAK to host
          982
031C D280        983          aksnd:  SETB    Closing
031E C282        984          CLR      PCRCV     ; turn PC LED on
0320 E52D        985          MOV      A,IDBUF   ; get local ID
0322 5407        986          ANL      A,#7      ; mask unused bits
0324 C4          987          SWAP    A          ; swap ID to upper IDS nibble
0325 252C        988          ADD      A,TXCNT   ; add retry count to IDS
0327 300B02      989          JNB     RAFLG,aks0 ; skip if not ACK
032A 2480        990          ADD      A,#128    ; else set ACK bit
032C F5F0        991          aks0:   MOV      B,A       ; hold IDS in B
032E E52E        992          MOV      A,TFBUF   ; get local TO/FROM
0330 C4          993          SWAP    A          ; switch TO and FROM
0331 C299        994          CLR      TI0       ; clear TI0 flag
0333 7599C0      995          MOV      SBUF0,#FEND ; send first FEND
0336 3099FD      996          aks1:   JNB     TI0,aks1 ; wait until byte sent
0339 C299        997          CLR      TI0       ; clear TI0 flag
033B 759910      998          MOV      SBUF0,#AKT ; send ACK type byte
033E 3099FD      999          aks2:   JNB     TI0,aks2 ; wait until byte sent
0341 C299        1000          CLR      TI0       ; clear TI0 flag
0343 F599        1001          MOV      SBUF0,A    ; send TO/FROM
0345 3099FD      1002          aks3:   JNB     TI0,aks3 ; wait until byte sent
0348 C299        1003          CLR      TI0       ; clear TI0 flag
034A 85F099      1004          MOV      SBUF0,B    ; send IDS
034D 3099FD      1005          aks4:   JNB     TI0,aks4 ; wait until byte sent
0350 C299        1006          CLR      TI0       ; clear TI0 flag
0352 7599C0      1007          MOV      SBUF0,#FEND ; send 2nd FEND
0355 3099FD      1008          aks5:   JNB     TI0,aks5 ; wait until byte sent
0358 C282        1009          clr     RFRCV     ; turn FCS LED off
035A D282        1010          SETB    PCRCV     ; turn PC LED off
035C C280        1011          CLR      Closing
035E 22          1012          aks_d:  RET          ; send ACK message done
          1013
          1014          ; delay to show FCS LED
          1015
035F 75F000      1016          led:   MOV      B,#0 ; load delay value
0362 7C58        1017          MOV          ;
0364 00          1018          led0:  NOP          ; NOP delay
0365 00          1019          NOP          ; NOP delay
0366 00          1020          NOP          ; NOP delay
0367 00          1021          NOP          ; NOP delay
0368 D5F0F9      1022          DJNZ    B,led0    ; loop to delay
036B DCF7        1023          DJNZ    r4,led0
036D 22          1024          led_d:  RET
          1025
          1026          ;*****
          1027
036E 75F000      1028          wait:  MOV      B,#0 ; load delay value

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0371 7C08      1029      MOV                      r4,#8
0373 00        1030      wait0:  NOP                ; NOP delay
0374 00        1031      NOP                    ; NOP delay
0375 00        1032      NOP                    ; NOP delay
0376 00        1033      NOP                    ; NOP delay
0377 D5F0F9    1034      DJNZ      B,wait0      ; loop to delay
037A DCF7      1035      DJNZ      r4,wait0
037C 22        1036      wait_d:  RET
1037
1038
1039      ; reset receive state, set SIHLD
1040
037D E4        1041      rxrst:  CLR      A                ; clear A
037E F517      1042      MOV      RXBH,A           ; clear buffer
0380 F516      1043      MOV      RXBL,A           ; clear buffer
0382 F518      1044      MOV      RXBB,A           ; clear buffer
0384 F519      1045      MOV      RMBYC,A          ; clear RX byte count
0386 F51C      1046      MOV      RMFCC,A          ; clear loop counter
0388 7861      1047      MOV      R0,#LNRX         ; point R0 to message start
038A C207      1048      CLR      OKFLG            ; clear FCS OK flag
038C C21A      1049      CLR      THFLG            ; clear TO here flag
038E C20C      1050      CLR      RMFLG            ; clear RF message flag
0390 C20D      1051      CLR      RCFLG            ; clear RF command flag
0392 C204      1052      CLR      SOPFLG           ; enable SOP test
0394 D208      1053      SETB    SIHLD             ; take serial in off hold
0396 C282      1054      clr      RFRCV            ; turn FCS LED off
0398 C283      1055      clr      RXI              ; turn RXI LED off
039A 22        1056      rxr_d:  RET                ; RX reset done
1057
1058      ; build FCS from each received byte
1059
039B 75F008    1060      b_rfcs:  MOV      B,#8        ; load loop count of 8
039E C3        1061      brf0:   CLR      C                ; clear carry bit
039F E51A      1062      MOV      A,RMFCS          ; load RX message byte
03A1 13        1063      RRC      A                ; shift lsb into carry
03A2 F51A      1064      MOV      A,RMFCS,A        ; store shifted message byte
03A4 9206      1065      MOV      FCSB,C           ; load FCSB with lsb
03A6 C3        1066      CLR      C                ; clear carry bit
03A7 EB        1067      MOV      A,R3             ; load high FCS byte
03A8 13        1068      RRC      A                ; shift right
03A9 FB        1069      MOV      R3,A             ; store shifted high FCS
03AA EF        1070      MOV      A,R7             ; load low FCS byte
03AB 13        1071      RRC      A                ; shift and pull in bit for FCS high
03AC FF        1072      MOV      R7,A             ; store shifted low FCS
03AD 300601    1073      JNB     FCSB,brf1         ; if lsb of low FCS = 0, jump to brf1
03B0 B3        1074      CPL      C                ; else complement carry bit
03B1 5008      1075      brf1:   JNC      brf2         ; if FCSB XOR (low FCS lsb) = 0 jump to brf2
03B3 EB        1076      MOV      A,R3             ; else load high FCS
03B4 6484      1077      XRL     A,#FCSSH          ; and XOR with high FCS poly
03B6 FB        1078      MOV      R3,A             ; store high FCS
03B7 EF        1079      MOV      A,R7             ; load low FCS
03B8 6408      1080      XRL     A,#FCSSL          ; XOR with low FCS poly
03BA FF        1081      MOV      R7,A             ; store low FCS
03BB D5F0E0    1082      brf2:   DJNZ     B,brf0      ; loop through bits in message byte
03BE 22        1083      brfcs_d:  RET                ; done this pass
1084
1085      ; test received message FCS
1086
03BF EB        1087      a_rfcs:  MOV      A,R3             ; load FCS high
03C0 B4F008    1088      CJNE    A,#FCVH,arf0      ; jump if not 0F0H
03C3 EF        1089      MOV      A,R7             ; load FCS low
03C4 B4B804    1090      CJNE    A,#FCVL,arf0      ; jump if not 0B8H
03C7 D282      1091      setb    RFRCV            ; else turn FCS LED on
03C9 D207      1092      SETB    OKFLG            ; set FCS OK flag
03CB 7BFF      1093      arf0:   MOV      R3,#FCSS        ; reseed FCS high
03CD 7FFF      1094      MOV      R7,#FCSS        ; reseed FCS low

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03CF 22          1095  arfcs_d: RET          ; RX FCS done
                  1096
                  1097
                  1098      ; RangeTest message (timer activated, host not required)
                  1099
03D0 201216     1100  do_ra:  JB      TXFLG,ra_d    ; skip is TX active
03D3 C200       1101          CLR      DCRON             ; idle RX DCR
03D5 C282       1102          CLR      PCRCV             ; PCRCV LED on
03D7 D282       1103          SETB     Open
03D9 F12D       1104          ACALL    hello2            ; get RangeTest message
03DB B111       1105          ACALL    txfcs             ; build and add FCS
03DD D282       1106          SETB     PCRCV             ; PCRCV LED off
03DF B129       1107          ACALL    txmsg             ; send TX message
03E1 B1BA       1108          ACALL    txrst             ; reset TX (retry)
03E3 C217       1109          CLR      RSFLG             ; clear RangeTest msg flag
03E5 D200       1110          SETB     DCRON             ; enable RX DCR
03E7 C282       1111          CLR      Open
03E9 22         1112  ra_d:  RET          ; RangeTest message done
                  1113
                  1114      ; get message from host, do command or transmit once
                  1115
03EA C282       1116  do_ht:  CLR      PCRCV             ; turn PC LED on
03EC C200       1117          CLR      DCRON             ; idle RX DCR
03EE 9135       1118          ACALL    htget             ; get message from host
03F0 918A       1119          ACALL    httyp             ; determine message type
03F2 301104     1120          JNB     HCFLG,ht0         ; skip if not host command
03F5 91B4       1121          ACALL    htcmd             ; else do command
03F7 810A       1122          AJMP    ht3               ; and enable DCR
03F9 30100A     1123  ht0:   JNB     HTFLG,ht1     ; skip if not transfer type
03FC B111       1124          ACALL    txfcs             ; else build and add FCS
03FE B129       1125          ACALL    txmsg             ; send TX message
0400 D212       1126          SETB     TXFLG             ; set TX active flag
0402 052C       1127          INC     TXCNT             ; increment TX count
0404 8108       1128          AJMP    ht2               ; and reset TX
0406 D20E       1129  ht1:   SETB     SIFLG         ; set SIFLG if unknown type
0408 B1BA       1130  ht2:   ACALL    txrst             ; reset TX (retry)
040A D200       1131  ht3:   SETB     DCRON             ; enable RX DCR
040C D282       1132          SETB     PCRCV             ; turn PC LED off
040E 22         1133  ht_d:  RET          ; TX message done
                  1134
                  1135      ; ping message once
                  1136
040F C282       1137  do_pi:  CLR      PCRCV             ; turn PC LED on
0411 C200       1138          CLR      DCRON             ; idle RX DCR
0413 B111       1139          ACALL    txfcs             ; build and add FCS
0415 B129       1140          ACALL    txmsg             ; send TX message
0417 D212       1141          SETB     TXFLG             ; set TX active flag
0419 052C       1142          INC     TXCNT             ; increment TX count
041B B1BA       1143          ACALL    txrst             ; reset TX (retry)
041D C219       1144          CLR      PMFLG             ; clear ping msg flag
041F D200       1145          SETB     DCRON             ; enable RX DCR
0421 D282       1146          SETB     PCRCV             ; turn PC LED off
0423 22         1147  pi_d:  RET          ; TX message done
                  1148
                  1149      ; transmit message again
                  1150
0424 C282       1151  do_rt:  CLR      PCRCV             ; else turn PCRCV LED on
0426 C200       1152          CLR      DCRON             ; idle RX DCR
0428 B129       1153          ACALL    txmsg             ; send TX message
042A 052C       1154          INC     TXCNT             ; increment TX count
042C B1BA       1155          ACALL    txrst             ; reset TX (retry)
042E C213       1156          CLR      TMFLG             ; clear TX msg flag
0430 D200       1157          SETB     DCRON             ; enable RX DCR
0432 D282       1158          SETB     PCRCV             ; turn PC LED off
0434 22         1159  rt_d:  RET          ; TX message done
                  1160

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1161      ; get message from host, clear SIFLG if valid
1162
0435 E599 1163 htget:  MOV     A,SBUF0      ; get byte
0437 C298 1164      CLR     RI0           ; clear RI flag
0439 B4C048 1165      CJNE    A,#FEND,htg8   ; done if not FEND
043C 7941 1166      MOV     R1,#LNTX      ; reset TX buffer index
043E F7    1167      MOV     @R1,A          ; store first FEND
043F 09    1168      INC     R1            ; bump TX buffer index
0440 0526 1169      INC     TMBYC         ; bump TX byte counter
0442 751E00 1170 htg0:  MOV     TMFCC,#0        ; reset timeout counter
0445 D20F 1171      SETB    TOFLG         ; set timeout flag
0447      1172 htg1:;  JNB     TOFLG,htg8     ; jump to htg8 if TOFLG resets
      1173 ;      JNB     RI0,htg1    ; else loop until next byte
0447 E599 1174      MOV     A,SBUF0      ; get byte
0449 C298 1175      CLR     RI0           ; clear RI flag
044B F7    1176      MOV     @R1,A          ; store byte
044C 09    1177      INC     R1            ; bump TX buffer index
044D 0526 1178      INC     TMBYC         ; bump TX byte counter
044F B4C002 1179      CJNE    A,#FEND,htg2   ; skip if not FEND
0452 815B 1180      AJMP    htg3          ; else jump to htg3
0454 E526 1181 htg2:  MOV     A,TMBYC         ; load A with number of bytes + 1
0456 B41DE9 1182      CJNE    A,#29,htg0     ; loop again if not 29th byte
0459 77C0 1183      MOV     @R1,#FEND     ; else force 2nd FEND
045B 7941 1184 htg3:  MOV     R1,#LNTX      ; reset TX buffer index
045D E526 1185      MOV     A,TMBYC         ; get byte count
045F B40202 1186      CJNE    A,#2,htg4      ; if not 2 jump to htg4
0462 8184 1187      AJMP    htg8          ; else jump to htg8
0464 C20E 1188 htg4:  CLR     SIFLG         ; disable serial in
0466 C20F 1189      CLR     TOFLG         ; clear timeout flag
0468 C299 1190      CLR     TI0           ; clear TI0 flag
046A 7599C0 1191      MOV     SBUF0,#FEND    ; send first FEND
046D 3099FD 1192 htg5:  JNB     TI0,htg5     ; wait until byte sent
0470 C299 1193      CLR     TI0           ; clear TI0 flag
0472 759906 1194      MOV     SBUF0,#6       ; send TACK byte
0475 3099FD 1195 htg6:  JNB     TI0,htg6     ; wait until byte sent
0478 C299 1196      CLR     TI0           ; clear TI0 flag
047A 7599C0 1197      MOV     SBUF0,#FEND    ; send 2nd FEND
047D 3099FD 1198 htg7:  JNB     TI0,htg7     ; wait until byte sent
0480 C299 1199      CLR     TI0           ; clear TI0 flag
0482 8189 1200      AJMP    htg_d         ; jump to done
0484 7941 1201 htg8:  MOV     R1,#LNTX      ; reset TX buffer index
0486 752600 1202      MOV     TMBYC,#0       ; reset byte counter
0489 22    1203 htg_d:  RET                ; get TX message done
1204
1205      ; determine host message type; update T/F if transfer
1206
048A E526 1207 http:  MOV     A,TMBYC         ; get message length
048C 6025 1208      JZ      htt_d         ; 0 not valid, done
048E E542 1209      MOV     A,TPTX         ; get host type byte
0490 54F0 1210      ANL     A,#240         ; mask out lower nibble, get type
0492 B44006 1211      CJNE    A,#HTCT,htt0   ; jump to htt0 if not host command
0495 C210 1212      CLR     HTFLG         ; clear host transfer flag
0497 D211 1213      SETB    HCFLG         ; set host command flag
0499 81B3 1214      AJMP    htt_d         ; done
049B 6420 1215 htt0:  XRL     A,#MSGT        ; compare with RF message type
049D 600A 1216      JZ      htt1          ; jump to htt1 if message
049F E542 1217      MOV     A,TPTX         ; get host type byte
04A1 54F0 1218      ANL     A,#240         ; mask out lower nibble, get type
04A3 6480 1219      XRL     A,#RXCT        ; compare with RF command type
04A5 6002 1220      JZ      htt1          ; jump to htt1 if RF command
04A7 81B3 1221      AJMP    htt_d         ; done
04A9 85432E 1222 htt1:  MOV     TFBUF,TFTX     ; update local TO/FROM buffer
04AC 85442D 1223      MOV     IDBUF,IDTX     ; update local ID buffer
04AF D210 1224      SETB    HTFLG         ; set host RF traffic flag
04B1 C211 1225      CLR     HCFLG         ; clear host command flag
04B3 22    1226 htg_d:  RET

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1227
1228 ; ACK host, do command, set SIFLG if not TX
1229
04B4 91D3 1230 htcmd: ACALL akhcm ; send host command ACK
04B6 D282 1231 setb RFRCV ; flash RFRCV & RXI
04B8 D283 1232 setb RXI ; to demo a command
04BA 7400 1233 MOV A,#0 ; outer delay value
04BC 75F000 1234 htc0: MOV B,#0 ; inner delay value
04BF 00 1235 htc1: NOP ; NOP to delay
04C0 00 1236 NOP ; NOP to delay
04C1 00 1237 NOP ; NOP to delay
04C2 D5F0FA 1238 DJNZ B,htc1 ; inner delay loop
04C5 D5E0F4 1239 DJNZ ACC,htc0 ; outer delay loop
04C8 715F 1240 ACALL led
04CA C282 1241 clr RFRCV ; turn off RFRCV
04CC C283 1242 clr RXI ; and RXI
04CE D20E 1243 htc2: SETB SIFLG ; TX enable host
04D0 C211 1244 htc3: CLR HCFLG ; reset host command flag
04D2 22 1245 htc_d: RET
1246
1247 ; ACK host command
1248
04D3 C282 1249 akhcm: CLR PCRCV ; turn ON PCRCV
04D5 E52D 1250 MOV A,IDBUF ; get local ID
04D7 5407 1251 ANL A,#7 ; mask unused bits
04D9 C4 1252 SWAP A ; swap ID to upper IDS nibble
04DA 2401 1253 ADD A,#1 ; add count to IDS
04DC 2480 1254 ADD A,#128 ; set ACK bit
04DE F5F0 1255 akh0: MOV B,A ; hold IDS in B
04E0 E52E 1256 MOV A,TFBUF ; get local TO/FROM
04E2 C4 1257 SWAP A ; switch TO and FROM
04E3 C299 1258 CLR TI0 ; clear TI0 flag
04E5 7599C0 1259 MOV SBUF0,#FEND ; send first FEND
04E8 3099FD 1260 akh1: JNB TI0,akh1 ; wait until byte sent
04EB C299 1261 CLR TI0 ; clear TI0 flag
04ED 759910 1262 MOV SBUF0,#ACKT ; send ACK type byte
04F0 3099FD 1263 akh2: JNB TI0,akh2 ; wait until byte sent
04F3 C299 1264 CLR TI0 ; clear TI0 flag
04F5 F599 1265 MOV SBUF0,A ; send TO/FROM
04F7 3099FD 1266 akh3: JNB TI0,akh3 ; wait until byte sent
04FA C299 1267 CLR TI0 ; clear TI0 flag
04FC 85F099 1268 MOV SBUF0,B ; send IDS
04FF 3099FD 1269 akh4: JNB TI0,akh4 ; wait until byte sent
0502 C299 1270 CLR TI0 ; clear TI0 flag
0504 7599C0 1271 MOV SBUF0,#FEND ; send 2nd FEND
0507 3099FD 1272 akh5: JNB TI0,akh5 ; wait until byte sent
050A C299 1273 CLR TI0 ; clear TI0 flag
050C C298 1274 CLR RI0 ; clear RI flag
050E D282 1275 SETB PCRCV ; turn OFF PCRCV
0510 22 1276 akh_d: RET ; host command ACK done
1277
1278 ; build FCS for transmit
1279
0511 0526 1280 txfcs: INC TMBYC ; number of bytes + 2 (FCS 2 bytes)
0513 A726 1281 MOV @R1,TMBYC ; replace FEND with number of bytes
0515 85261E 1282 MOV TMFCC,TMBYC ; move byte count to loop counter
0518 151E 1283 DEC TMFCC ; loop count is 2 less than
051A 151E 1284 DEC TMFCC ; number of bytes including FCS
051C 8729 1285 txf0: MOV TMFCS,@R1 ; get next message byte
051E 09 1286 INC R1 ; bump pointer
051F B1D1 1287 ACALL b_tfcs ; build FCS
0521 D51EF8 1288 DJNZ TMFCC,txf0 ; loop for next byte
0524 B1F5 1289 ACALL a_tfcs ; add FCS
0526 7941 1290 MOV R1,#LNTX ; reset TX message pointer
0528 22 1291 txf_d: RET ; TX FCS done
1292

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```

1293 ; transmit preamble, SOP and message
1294
0529 D1F9 1295 txmsg: CALL tx_on ; spi command to
rf

ic
1296
1297 ; clr CL1 ; turn TX on
052B 75F064 1298 MOV B,#100 ; load TX delay count
052E D5F0FD 1299 txp0: DJNZ B,txp0 ; loop to delay
0531 900775 1300 MOV DPTR,#tstrt ; point to start symbol table
0534 751D00 1301 MOV TXSI,#0 ; clear index
0537 75F006 1302 MOV B,#6 ; load 6 into loop counter
053A 751F00 1303 MOV TXSMC,#0 ; load 0 into sample count (fall through)
053D D214 1304 SETB TSFLG ; flag to output TX samples
053F E51D 1305 txs0: MOV A,TXSI ; load index into A
0541 051D 1306 INC TXSI ; increment index
0543 93 1307 MOVC A,@+DPTR ; load table entry
0544 F525 1308 MOV TMBYT,A ; into TMBYT
0546 752408 1309 MOV TMBIC,#8 ; load 8 into bit counter
0549 E525 1310 txs1: MOV A,TMBYT ; load start symbol byte into A
054B 33 1311 RLC A ; shift bit left into carry
054C F525 1312 MOV TMBYT,A ; store shifted message byte
054E E51F 1313 txs2: MOV A,TXSMC ; get sample count
0550 70FC 1314 JNZ txs2 ; loop until 0 (synchronize with tick isr)
0552 9215 1315 MOV TXBIT,C ; load next TX bit
0554 751F03 1316 MOV TXSMC,#3 ; reload sample count
0557 D524EF 1317 DJNZ TMBIC,txs1 ; send 8 bits/byte
055A D5F0E2 1318 DJNZ B,txs0 ; send 6 bytes
055D 90077B 1319 txm0: MOV DPTR,#tx_smb1 ; point to symbol table;
0560 8526F0 1320 MOV B,TMBYC ; load B with byte count
0563 E7 1321 txm1: MOV A,@R1 ; get TX message byte
0564 09 1322 INC R1 ; bump message index
0565 F525 1323 MOV TMBYT,A ; copy byte into TMBYT
0567 540F 1324 ANL A,#0FH ; mask upper nibble
0569 93 1325 MOVC A,@+DPTR ; get 6-bit symbol
056A F527 1326 MOV TXSL,A ; move to TXSL
056C E525 1327 MOV A,TMBYT ; get TMBYT
056E C4 1328 SWAP A ; swap nibbles
056F 540F 1329 ANL A,#0FH ; mask swapped lower nibble
0571 93 1330 MOVC A,@+DPTR ; get 6-bit symbol
0572 F528 1331 MOV TXSH,A ; move to TXSH
0574 75240C 1332 MOV TMBIC,#12 ; set bit count to 12
0577 E524 1333 txm2: MOV A,TMBIC ; get bit count
0579 C3 1334 CLR C ; clear carry
057A 9407 1335 SUBB A,#7 ; subtract 7
057C 4007 1336 JC txm3 ; if < 7 jump to txm3
057E E528 1337 MOV A,TXSH ; get high TX symbol
0580 33 1338 RLC A ; shift left into carry
0581 F528 1339 MOV TXSH,A ; store shifted message byte
0583 A18A 1340 AJMP txm4 ; jump to txm4
0585 E527 1341 txm3: MOV A,TXSL ; get low TX symbol
0587 33 1342 RLC A ; shift left into carry
0588 F527 1343 MOV TXSL,A ; store shifted message byte
058A E51F 1344 txm4: MOV A,TXSMC ; get sample count
058C 70FC 1345 JNZ txm4 ; loop until 0 (synchronize with tick isr)
058E 9215 1346 MOV TXBIT,C ; load next bit
0590 751F03 1347 MOV TXSMC,#3 ; reload sample count
0593 1524 1348 DEC TMBIC ; decrement bit count
0595 E524 1349 MOV A,TMBIC ; get TMBIC
0597 6002 1350 JZ txm5 ; if 0 jump to txm5
0599 A177 1351 AJMP txm2 ; else loop again
059B D5F0C5 1352 txm5: DJNZ B,txm1 ; loop to send next byte
059E E51F 1353 txm6: MOV A,TXSMC ; get sample count
05A0 70FC 1354 JNZ txm6 ; loop until 0 (synchronize with tick isr)
05A2 C214 1355 CLR TSFLG ; clear TX sample out flag
05A4 C293 1356 CLR TXPIN ; clear TX out pin
05A6 F104 1357 CALL tx_off

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```

; spi commnad to rfic
1358 ;
1359 ; setb CL1 ; turn TX off
05A8 22 txm_d: RET ; TX message done
1360
1361 ; TX master reset
1362
05A9 C20B txmrs: CLR RAFLG ; reset RF ACK flag
05AB C20A CLR SNFLG ; reset TX NAK flag
05AD C212 CLR TXFLG ; reset TX active flag
05AF C21B CLR RHFLG ; reset repeat here flag
05B1 B1BA ACALL txrst ; full reset TX
05B3 D20E SETB SIFLG ; enable serial in
05B5 C299 CLR TI0 ; clear TI0 flag
05B7 C298 CLR RI0 ; clear RI flag
05B9 22 txs_d: RET ; master TX reset done
1372
1373
1374 ; reset transmit state (retry or full)
1375
05BA 7941 txrst: MOV R1,#LNTX ; point R1 to length byte
05BC E4 CLR A ; clear A to
05BD F525 MOV TMBYT,A ; clear TX message byte
05BF F51E MOV TMFCC,A ; clear TX FCS count
05C1 F51F MOV TXSMC,A ; clear TX sample count
05C3 F527 MOV TXSL,A ; clear TX symbol low
05C5 F528 MOV TXSH,A ; clear TX symbol high
05C7 201206 JB TXFLG,txr_d ; skip if TX active
1384
1385 ; full reset if TXFLG clear
1386
05CA F526 MOV TMBYC,A ; reset TX byte count
05CC F52C MOV TXCNT,A ; reset TX retry count
05CE F52B MOV TXTH,A ; clear TX timer high
05D0 22 txr_d: RET ; TX reset done
1391
1392 ; build transmit FCS from each byte
1393
05D1 75F008 b_tfcs: MOV B,#8 ; load loop count of 8
05D4 C3 btff0: CLR C ; clear carry bit
05D5 E529 MOV A,TMFCS ; load TX message byte
05D7 13 RRC A ; shift lsb into carry
05D8 F529 MOV TMFCS,A ; store shifted message byte
05DA 9206 MOV FCSB,C ; load FCSB with lsb
05DC C3 CLR C ; clear carry bit
05DD ED MOV A,R5 ; load high FCS byte
05DE 13 RRC A ; shift right
05DF FD MOV R5,A ; store shifted high FCS
05E0 EE MOV A,R6 ; load low FCS byte
05E1 13 RRC A ; shift and pull in bit for FCS high
05E2 FE MOV R6,A ; store shifted low FCS
05E3 300601 JNB FCSB,btff1 ; if lsb of low FCS = 0, jump to btff1
05E6 B3 CPL C ; else complement carry bit
05E7 5008 btff1: JNC btff2 ; if FCSB XOR (low FCS lsb) = 0 jump to btff2
05E9 ED MOV A,R5 ; else load high FCS
05EA 6484 XRL A,#FCSH ; and XOR with high FCS poly
05EC FD MOV R5,A ; store high FCS
05ED EE MOV A,R6 ; load low FCS
05EE 6408 XRL A,#FCSL ; XOR with low FCS poly
05FO FE MOV R6,A ; store low FCS
05F1 D5F0E0 btff2: DJNZ B,btff0 ; loop through bits in message byte
05F4 22 btffcs_d: RET ; done this pass
1418
1419 ; complement and append FCS
1420
05F5 EE a_tfcs: MOV A,R6 ; load FCS (high/low switch)
05F6 F4 CPL A ; 1's complement

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05F7 F7          1423          MOV      @R1,A          ; store at end of TX message
05F8 09          1424          INC      R1             ; increment TX message byte pointer
05F9 ED          1425          MOV      A,R5          ; load FCS (high/low switch)
05FA F4          1426          CPL      A             ; 1's complement
05FB F7          1427          MOV      @R1,A         ; store at end of TX message
05FC 7DFF        1428          MOV      R5,#FCSS     ; reseed FCS high
05FE 7EFF        1429          MOV      R6,#FCSS     ; reseed FCS low
0600 22          1430          atfcs_d: RET          ; add TX FCS done
                1431
                1432          ; initialize software
                1433
0601 C2AF        1434          setup:  CLR      EA             ; disable interrupts
0603 75D900      1435          set_ck: MOV      PCA0MD,#000H    ; disable watchdog
0606 75B283      1436          MOV      OSCICN,#083H    ; set SiLabs CPU clock to 24.5 MHz/ without is 3mhz...
0609 758E00      1437          MOV      CKCON,#000H    ; divide by 12 for timers 000
060C            1438          set_io:
060C 75A45F      1439          mov      P0MDOUT,#05Fh    ; was ff, 7f
060F 75A57B      1440          mov      P1MDOUT,#07Bh    ; was fb
0612 75E101      1441          mov      XBR0,#001h
0615 75E2C0      1442          mov      XBR1,#0C0h
                1443
0618            1444          new_io:
0618 75A4FF      1445          mov      P0MDOUT, #0FFh
061B 75A502      1446          mov      P1MDOUT, #002h
061E 75D40F      1447          mov      POSKIP, #00Fh
0621 75E103      1448          mov      XBR0, #003h
0624 75E240      1449          mov      XBR1, #040h
                1450
0627 75A45F      1451          mov      P0MDOUT, #05Fh
062A 75A503      1452          mov      P1MDOUT, #003h
062D 75D40F      1453          mov      POSKIP, #00Fh
0630 75E103      1454          mov      XBR0, #003h
0633 75E240      1455          mov      XBR1, #040h
                1456
                1457          ;*****
0636            1458          set_spio:
                1459
0636 75A170      1460          mov      SPIOCFG, #070h
0639 75F809      1461          mov      SPIOCN, #009h
063C 75A206      1462          mov      SPIOCKR, #006h
                1463
                1464
                1465          ;          setb      CL0          ; TR RX mode
                1466          ;          setb      CL1          ; TR RX mode
                1467
                1468          ;          mov      TMOD, #020h
                1469          ;          mov      CKCON, #008h
                1470          ;          mov      TH1, #0B1h
                1471
063F C293        1472          CLR      TXPIN          ; turn TX modulation off
0641 7816        1473          MOV      R0,#22         ; starting above stack
0643 75F06A      1474          MOV      B,#106        ; clear 106 bytes
0646 E4          1475          CLR      A             ; clear A
0647 F6          1476          clear:  MOV      @R0,A     ; clear flags, bytes and buffers
0648 08          1477          INC      R0             ; bump pointer
0649 D5F0FB      1478          DJNZ    B,clear        ; loop again
064C 758922      1479          tick_su: MOV      TMOD,#022H    ; set timers T0 and T1 to mode 2 022
064F C28C        1480          CLR      TR0           ; stop timer T0
0651 C28D        1481          CLR      TF0           ; clear T0 overflow
0653 758CE1      1482          MOV      TH0,#ITICK    ; load count for tick
0656 758AE1      1483          MOV      TL0,#ITICK    ; load count for tick
0659 D2B9        1484          SETB    PTO           ; give T0 first interrupt priority
065B D2A9        1485          SETB    ET0           ; unmask T0 interrupt
065D D28C        1486          SETB    TR0           ; start timer T0
065F C28E        1487          uart_su: CLR      TR1     ; stop timer T1
0661 C28F        1488          CLR      TF1           ; clear T1 overflow

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0663 758DCB      1489      MOV      TH1,#0CBH      ; load baud rate count for 19.2 kb/s 0cb
0666 758BCB      1490      MOV      TLL,#0CBH      ; load baud rate count for 19.2 kb/s 0cb
0669 759810      1491      MOV      SCON0,#010H    ; enable UART mode 1
066C C2AC        1492      CLR      ESO            ; mask serial interrupt
066E D28E        1493      SETB     TR1           ; start baud rate timer T1
0670 D208        1494      SETB     SIHLD         ; disable serial hold off (default)
0672 D20E        1495      SETB     SIFLG         ; enable serial in (default)
0674 F117        1496      ACALL    hello         ; send start up message
0676 7861        1497      buf_su: MOV      R0,#LNRX ; load RX buffer pointer
0678 7941        1498      MOV      R1,#LNTX     ; load TX buffer pointer
067A 7A00        1499      MOV      R2,#0        ; zero DCR ramp
067C 7BFF        1500      MOV      R3,#FCSS     ; seed R3
067E 7DFF        1501      MOV      R5,#FCSS     ; seed R5
0680 7EFF        1502      MOV      R6,#FCSS     ; seed R6
0682 7FFF        1503      MOV      R7,#FCSS     ; seed R7
0684 752E22      1504      MOV      TFBUF,#34    ; initialize TO/FROM 2 & 2
0687 752D00      1505      MOV      IDBUF,#0     ; initialize ID = 0
                                1506
068A A297        1507      rtst_su: MOV     C,ID0  ; read ID0
068C 4005        1508      JC       isr_on       ; skip if no ID0 jumper
068E D216        1509      SETB     RTFLG        ; else set RangeTest flag
0690 753102      1510      MOV      RTTH,#RTTM   ; load TX timer high
                                1511
                                1512
0693 C204        1513      isr_on: CLR      SOPFLG ; clear SOP detect flag
0695 D200        1514      SETB     DCRON        ; enable RX DCR
0697 D2AF        1515      SETB     EA           ; enable interrupts
0699 C299        1516      CLR      TI0          ; clear TI0 (serial byte sent) flag
069B C298        1517      CLR      RI0          ; clear RI (serial byte received) flag
069D 22         1518      setup_d: RET          ; setup done
                                1519
                                1520
                                ;*****
069E           1521      rfic:
069E 75A380      1522      mov      SPIODAT,      #080h

06A1 F10F        1523      ACALL    spio_wait
06A3 75A333      1524      mov      SPIODAT,      #033h
                                ;33 = 902, 23 = 868, 13 = 433
06A6 F10F        1525      ACALL    spio_wait
06A8 75A3A3      1526      mov      SPIODAT,      #0a3h

06AB F10F        1527      ACALL    spio_wait
06AD 75A363      1528      mov      SPIODAT,      #063h
06B0 F10F        1529      ACALL    spio_wait
06B2 75A392      1530      mov      SPIODAT,      #092h

06B5 F10F        1531      ACALL    spio_wait
06B7 75A380      1532      mov      SPIODAT,      #080h ;#080h ;#0
a0h, 060h = 270khz bw

06BA F10F        1533      ACALL    spio_wait
06BC 75A398      1534      mov      SPIODAT,      #098h

06BF F10F        1535      ACALL    spio_wait
06C1 75A360      1536      mov      SPIODAT,      #060h ;#060h ;#02
0h, 080h = 135k dev

06C4 F10F        1537      ACALL    spio_wait
06C6 75A3C4      1538      mov      SPIODAT,      #0c4h

06C9 F10F        1539      ACALL    spio_wait
06CB 75A367      1540      mov      SPIODAT,      #067h ;#067h
06CE F10F        1541      ACALL    spio_wait
06D0 75A3C6      1542      mov      SPIODAT,      #0c6h

06D3 F10F        1543      ACALL    spio_wait
06D5 75A311      1544      mov      SPIODAT,      #011h
06D8 F10F        1545      ACALL    spio_wait

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06DA 75A3C2      1546      mov          SPIODAT,      #0c2h

06DD F10F        1547      ACALL spio_wait
06DF 75A33C      1548      mov          SPIODAT,      #03ch
06E2 F10F        1549      ACALL spio_wait
06E4 75A382      1550      mov          SPIODAT,      #082h

06E7 F10F        1551      ACALL spio_wait
06E9 75A309      1552      mov          SPIODAT,      #009h
06EC F10F        1553      ACALL spio_wait
06EE 75A382      1554      mov          SPIODAT,      #082h

06F1 F10F        1555      ACALL spio_wait
06F3 75A319      1556      mov          SPIODAT,      #019h
06F6 F10F        1557      ACALL spio_wait
1558
06F8 22          1559      RET
1560
1561
1562
06F9            1563      ;*****
06F9 75A382      1564      tx_on:      mov          SPIODAT,      #082h
                                           ;SPIO = 82d9h to rfic, rx on tx off

06FC F10F        1565      ACALL spio_wait
06FE 75A339      1566      mov          SPIODAT,      #039h
0701 F10F        1567      ACALL spio_wait
0703 22          1568      RET
1569

0704            1570      tx_off:    mov          SPIODAT,      #082h
0704 75A382      1571      ;SPIO = 82d9h to rfic, rx on tx off
                                           ACALL spio_wait
0707 F10F        1572      mov          SPIODAT,      #0d9h
0709 75A3D9      1573      ACALL spio_wait
070C F10F        1574      mov          SPIODAT,      #0d9h
070E 22          1575      RET
1576

070F            1577      spio_wait:
070F E5F8        1578      mov     A,SPIOCN
0711 5402        1579      ANL     A,#02h
0713 B402F9      1580      cjne   a,#02h,spio_wait
0716 22          1581      RET
1582
1583      ;*****
1584
1585
1586
1587      ; send SW version to host
1588
0717 9007D3      1589      hello:    MOV     DPTR,#table      ; point to table
071A 75F00E      1590      MOV     B,#14             ; load loop count in B
071D 7F00        1591      MOV     R7,#0            ; R7 has first table entry
071F EF         1592      snd_h:   MOV     A,R7           ; move table offset into A
0720 93         1593      MOV     A,@A+DPTR        ; load table byte
0721 C299        1594      CLR     TI0              ; clear TI0 flag
0723 F599        1595      MOV     SBUF0,A          ; send byte
0725 3099FD      1596      nxt_tx:  JNB     TI0,nxt_tx    ; wait until sent
0728 0F         1597      INC     R7               ; bump index
0729 D5F0F3      1598      DJNZ   B,snd_h          ; loop to send message
072C 22          1599      hello_d: RET              ; done
1600
1601      ; load RangeTest message (not used in this SW version)
1602
072D            1603      hello2:
072D E538        1604      ;*****
072D E538        1605      MOV     A,fhss           ; load ID into A
072F 04         1606      INC     A                ; bump ID for next time

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0730 B41801      1607          cjne          a,#024,h1b
0733 E4          1608          clr          a
0734 F538        1609      h1b:      mov          fhss,a
0736 75A3A1      1610          mov          SPIODAT,#0A1h ; Sent MSB of f

          req

0739 F10F        1611          ACALL       spio_wait
073B AC38        1612          mov          R4,fhss
073D 0C          1613          inc          r4
073E E4          1614          clr          a
073F 240A        1615      h1:      add          a,#10
0741 DCFC        1616          djnz        r4,h1
0743 F5A3        1617          mov          SPIODAT,A      ; Send LSB of Fr

          eq

0745 F10F        1618          ACALL       spio_wait
0747 716E        1619          ACALL       wait
0749 716E        1620          ACALL       wait
074B 716E        1621          ACALL       wait
074C          1622          ;*****
074D          1623
074D 7941        1624          MOV          R1,#LNTX      ; reset TX buffer pointer
074F 9007E1      1625          MOV          DPTR,#tbl_2   ; point to table 2
0752 75F00F      1626          MOV          B,#15        ; load loop count in B
0755 752600      1627          MOV          TMBYC,#0     ; offset for first table entry
0758 E526        1628      snd_h2:  MOV          A,TMBYC      ; move table offset into A
075A 93          1629          MOVC        A,@A+DPTR     ; load table byte
075B F7          1630          MOV          @R1,A        ; into TX buffer
075C 0526        1631          INC          TMBYC        ; increment TMBYC
075E 09          1632          INC          R1          ; increment R1
075F D5F0F6      1633          DJNZ        B,snd_h2     ; loop to load message
0762 7941        1634          MOV          R1,#LNTX     ; reset TX pointer
0764 853044      1635          MOV          IDTX,RTID    ; get RangeTest ID
0767 E544        1636          MOV          A,IDTX       ; load ID into A
0769 04          1637          INC          A           ; bump ID for next time
076A B40701      1638          cjne        a,#7,h1a     ;
076D E4          1639          clr          a
076E F530        1640      h1a:      mov          RTID,a
0770 E538        1641          mov          a,fhss
0772 F545        1642          mov          CMTX,A
0773          1643
0774 22          1644      helo2_d: RET
0775          1645
0776          1646          ; tables:
0777          1647
0775 AA          1648      tstrt:  DB          170      ; preamble/SOP table
0776 AA          1649          DB          170      ; table data
0777 AA          1650          DB          170      ; table data
0778 AA          1651          DB          170      ; table data
0779 E2          1652          DB          226     ; table data
077A E2          1653          DB          226     ; table data
077B          1654
077B 34          1655      tx_smb1: DB          52      ; 4-to-6 TX table (flush left)
077C 38          1656          DB          56      ; table data
077D 4C          1657          DB          76      ; table data
077E 54          1658          DB          84      ; table data
077F 58          1659          DB          88      ; table data
0780 64          1660          DB          100     ; table data
0781 68          1661          DB          104     ; table data
0782 70          1662          DB          112     ; table data
0783 8C          1663          DB          140     ; table data
0784 94          1664          DB          148     ; table data
0785 98          1665          DB          152     ; table data
0786 A4          1666          DB          164     ; table data
0787 A8          1667          DB          168     ; table data
0788 B0          1668          DB          176     ; table data
0789 C8          1669          DB          200     ; table data
078A D0          1670          DB          208     ; table data

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1671
078B FF 1672 rx_smb1: DB 255 ; 6-to-4 RX table (flush right)
078C FF 1673 DB 255 ; table data
078D FF 1674 DB 255 ; table data
078E FF 1675 DB 255 ; table data
078F FF 1676 DB 255 ; table data
0790 FF 1677 DB 255 ; table data
0791 FF 1678 DB 255 ; table data
0792 FF 1679 DB 255 ; table data
0793 FF 1680 DB 255 ; table data
0794 FF 1681 DB 255 ; table data
0795 FF 1682 DB 255 ; table data
0796 FF 1683 DB 255 ; table data
0797 FF 1684 DB 255 ; table data
0798 00 1685 DB 0 ; table data
0799 01 1686 DB 1 ; table data
079A FF 1687 DB 255 ; table data
079B FF 1688 DB 255 ; table data
079C FF 1689 DB 255 ; table data
079D FF 1690 DB 255 ; table data
079E 02 1691 DB 2 ; table data
079F FF 1692 DB 255 ; table data
07A0 03 1693 DB 3 ; table data
07A1 04 1694 DB 4 ; table data
07A2 FF 1695 DB 255 ; table data
07A3 FF 1696 DB 255 ; table data
07A4 05 1697 DB 5 ; table data
07A5 06 1698 DB 6 ; table data
07A6 FF 1699 DB 255 ; table data
07A7 07 1700 DB 7 ; table data
07A8 FF 1701 DB 255 ; table data
07A9 FF 1702 DB 255 ; table data
07AA FF 1703 DB 255 ; table data
07AB FF 1704 DB 255 ; table data
07AC FF 1705 DB 255 ; table data
07AD FF 1706 DB 255 ; table data
07AE 08 1707 DB 8 ; table data
07AF FF 1708 DB 255 ; table data
07B0 09 1709 DB 9 ; table data
07B1 0A 1710 DB 10 ; table data
07B2 FF 1711 DB 255 ; table data
07B3 FF 1712 DB 255 ; table data
07B4 0B 1713 DB 11 ; table data
07B5 0C 1714 DB 12 ; table data
07B6 FF 1715 DB 255 ; table data
07B7 0D 1716 DB 13 ; table data
07B8 FF 1717 DB 255 ; table data
07B9 FF 1718 DB 255 ; table data
07BA FF 1719 DB 255 ; table data
07BB FF 1720 DB 255 ; table data
07BC FF 1721 DB 255 ; table data
07BD 0E 1722 DB 14 ; table data
07BE FF 1723 DB 255 ; table data
07BF 0F 1724 DB 15 ; table data
07C0 FF 1725 DB 255 ; table data
07C1 FF 1726 DB 255 ; table data
07C2 FF 1727 DB 255 ; table data
07C3 FF 1728 DB 255 ; table data
07C4 FF 1729 DB 255 ; table data
07C5 FF 1730 DB 255 ; table data
07C6 FF 1731 DB 255 ; table data
07C7 FF 1732 DB 255 ; table data
07C8 FF 1733 DB 255 ; table data
07C9 FF 1734 DB 255 ; table data
07CA FF 1735 DB 255 ; table data
1736

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1737 ; TX retry delay values (34.73 us tick)
1738
07CB 07 1739 delay: DB 7 ; 0.062 second
07CC 0F 1740 DB 15 ; 0.133 second
07CD 0B 1741 DB 11 ; 0.098 second
07CE 14 1742 DB 20 ; 0.178 second
07CF 09 1743 DB 9 ; 0.080 second
07D0 12 1744 DB 18 ; 0.160 second
07D1 0D 1745 DB 13 ; 0.116 second
07D2 16 1746 DB 22 ; 0.196 second
1747
07D3 20 1748 table: DB ' ' ; Start-Up message
07D4 20 1749 DB 32 ; table data
07D5 22 1750 DB 34 ; table data
07D6 52 1751 DB 'R' ; table data
07D7 46 1752 DB 'F' ; table data
07D8 4D 1753 DB 'M' ; table data
07D9 20 1754 DB ' ' ; table data
07DA 20 1755 DB ' ' ; table data
07DB 52 1756 DB 'R' ; table data
07DC 46 1757 DB 'F' ; table data
07DD 49 1758 DB 'I' ; table data
07DE 43 1759 DB 'C' ; table data
07DF 20 1760 DB ' ' ; table data
07E0 20 1761 DB ' ' ; table data
1762
07E1 C0 1763 tbl_2: DB 192 ; RangeTest message
07E2 20 1764 DB 32 ; table data
07E3 22 1765 DB 34 ; table data
07E4 30 1766 DB '0' ; table data
07E5 31 1767 DB '1' ; table data
07E6 46 1768 DB 'F' ; table data
07E7 48 1769 DB 'H' ; table data
07E8 53 1770 DB 'S' ; table data
07E9 53 1771 DB 'S' ; table data
07EA 20 1772 DB ' ' ; table data
07EB 54 1773 DB 'T' ; table data
07EC 65 1774 DB 'e' ; table data
07ED 73 1775 DB 's' ; table data
07EE 74 1776 DB 't' ; table data
07EF 20 1777 DB ' ' ; table data
07F0 20 1778 DB ' ' ; table data
1779
1780
1781
1782 END ; end of source code

```

XREF SYMBOL TABLE LISTING

N A M E	T Y P E	V A L U E	ATTRIBUTES / REFERENCES
AC	B ADDR	00D0H.6 A	246#
ACC	D ADDR	00E0H A	160# 474 504 528 612 1239
ACK	B ADDR	00C0H.1 A	232#
ACKRQ	B ADDR	00C0H.3 A	230#
ACKRX	C ADDR	0261H A	866#
ACKT	N NUMB	0010H A	324# 855 872 873 998 1262
AD0BUSY	B ADDR	00E8H.4 A	265#
AD0CM0	B ADDR	00E8H.0 A	269#
AD0CM1	B ADDR	00E8H.1 A	268#
AD0CM2	B ADDR	00E8H.2 A	267#
AD0EN	B ADDR	00E8H.7 A	262#
AD0INT	B ADDR	00E8H.5 A	264#
AD0TM	B ADDR	00E8H.6 A	263#
AD0WINT	B ADDR	00E8H.3 A	266#
ADCOCF	D ADDR	00BCH A	136#
ADCOCN	D ADDR	00E8H A	166#
ADCOGTH	D ADDR	00C4H A	143#
ADCOGTL	D ADDR	00C3H A	142#
ADCOH	D ADDR	00BEH A	138#
ADCOL	D ADDR	00BDH A	137#
ADCOLTH	D ADDR	00C6H A	145#
ADCOLTL	D ADDR	00C5H A	144#
AD_D	C ADDR	02EBH A	947#
AD_TX	C ADDR	02DBH A	775 940#
AKH0	C ADDR	04DEH A	1255#
AKH1	C ADDR	04E8H A	1260# 1260
AKH2	C ADDR	04F0H A	1263# 1263
AKH3	C ADDR	04F7H A	1266# 1266
AKH4	C ADDR	04FFH A	1269# 1269
AKH5	C ADDR	0507H A	1272# 1272
AKHCM	C ADDR	04D3H A	1230 1249#
AKH_D	C ADDR	0510H A	1276#
AKS0	C ADDR	032CH A	989 991#
AKS1	C ADDR	0336H A	996# 996
AKS2	C ADDR	033EH A	999# 999
AKS3	C ADDR	0345H A	1002# 1002
AKS4	C ADDR	034DH A	1005# 1005
AKS5	C ADDR	0355H A	1008# 1008
AKSND	C ADDR	031CH A	721 742 983#
AKS_D	C ADDR	035EH A	1012#
AMXON	D ADDR	00BAH A	134#
AMXOP	D ADDR	00BBH A	135#
ARBLOST	B ADDR	00C0H.2 A	231#
ARF0	C ADDR	03CBH A	1088 1090 1093#
ARFCS_D	C ADDR	03CFH A	1095#
ARX0	C ADDR	02A0H A	899#
ARX_D	C ADDR	02A4H A	901#
ATFCS_D	C ADDR	0600H A	1430#
A_RFCS	C ADDR	03BFH A	826 1087#
A_TFCS	C ADDR	05F5H A	887 1289 1421#
B	D ADDR	00F0H A	172# 833 837 991 1004 1016 1022 1028 1034 1060 1082 1234 1238 1255 1268 1298 1299 1302 1318 1320 1352 1394 1416 1474 1478 1590 1598 1626 1633
BRF0	C ADDR	039EH A	1061# 1082
BRF1	C ADDR	03B1H A	1073 1075#
BRF2	C ADDR	03BBH A	1075 1082#
BRFCS_D	C ADDR	03BEH A	1083#
BTF0	C ADDR	05D4H A	1395# 1416
BTF1	C ADDR	05E7H A	1407 1409#
BTF2	C ADDR	05F1H A	1409 1416#
BTFCS_D	C ADDR	05F4H A	1417#

BUF01.	N NUMB	0032H	A	432#
BUF02.	N NUMB	0033H	A	433#
BUF03.	N NUMB	0034H	A	434#
BUF04.	N NUMB	0035H	A	435#
BUF05.	N NUMB	0036H	A	436# 594
BUF06.	N NUMB	0037H	A	437# 595 598 608
BUF_SU	C ADDR	0676H	A	1497#
B_RFCS	C ADDR	039BH	A	824 1060#
B_TFCS	C ADDR	05D1H	A	870 874 880 885 1287 1394#
CCF0	B ADDR	00D8H.0	A	259#
CCF1	B ADDR	00D8H.1	A	258#
CCF2	B ADDR	00D8H.2	A	257#
CF	B ADDR	00D8H.7	A	255#
CHAN	C ADDR	00F0H	A	617#
CHAN0.	C ADDR	010AH	A	638#
CKCON.	D ADDR	008EH	A	102# 1437
CL0	B ADDR	0090H.0	A	444#
CL1	B ADDR	0090H.1	A	443#
CLEAR.	C ADDR	0647H	A	1476# 1478
CLKSEL	D ADDR	00A9H	A	125#
CLOSED	B ADDR	0080H.3	A	458# 606 659 671
CLOSING.	B ADDR	0080H.0	A	461# 596 599 605 665 677 983 1011
CMRX	N NUMB	0065H	A	310# 752 905
CMTX	N NUMB	0045H	A	302# 1642
CPT0CN	D ADDR	009BH	A	114#
CPT0MD	D ADDR	009DH	A	115#
CPT0MX	D ADDR	009FH	A	116#
CR	B ADDR	00D8H.6	A	256#
CY	B ADDR	00D0H.7	A	245#
DCR	C ADDR	0012H	A	479#
DCR0	C ADDR	001AH	A	483#
DCR1	C ADDR	001EH	A	483 485#
DCR2	C ADDR	0024H	A	485 488#
DCR3	C ADDR	002EH	A	489 493#
DCR4	C ADDR	0035H	A	492 496#
DCR5	C ADDR	0041H	A	503 505#
DCR6	C ADDR	0063H	A	496 524#
DCR7	C ADDR	006CH	A	527 529#
DCRON.	N NUMB	0000H	A	351# 475 733 782 1101 1110 1117 1131 1138 1145 1152 1157 1514
DCR_D.	C ADDR	007CH	A	487 493 495 509 511 519 530 535#
DELAY.	C ADDR	07CBH	A	579 1739#
DO_HT.	C ADDR	03EAH	A	717 1116#
DO_PI.	C ADDR	040FH	A	727 1137#
DO_RA.	C ADDR	03D0H	A	711 1100#
DO_RT.	C ADDR	0424H	A	719 1151#
DO_RX.	C ADDR	017DH	A	725 732#
DPH	D ADDR	0083H	A	94#
DPL	D ADDR	0082H	A	93#
EA	B ADDR	00A8H.7	A	207# 1434 1515
EIE1	D ADDR	00E6H	A	165#
EIP1	D ADDR	00F6H	A	175#
EMIOCN	D ADDR	00AAH	A	126#
ES0	B ADDR	00A8H.4	A	210# 1492
ESPI0.	B ADDR	00A8H.6	A	208#
ET0	B ADDR	00A8H.1	A	213# 1485
ET1	B ADDR	00A8H.3	A	211#
ET2	B ADDR	00A8H.5	A	209#
EX0	B ADDR	00A8H.0	A	214#
EX1	B ADDR	00A8H.2	A	212#
F0	B ADDR	00D0H.5	A	247#
F1	B ADDR	00D0H.1	A	251#
FCSB	N NUMB	0006H	A	357# 1065 1073 1399 1407
FCSH	N NUMB	0084H	A	342# 1077 1411
FCSL	N NUMB	0008H	A	343# 1080 1414
FCSS	N NUMB	00FFH	A	341# 1093 1094 1428 1429 1500 1501 1502 1503
FCVH	N NUMB	00F0H	A	344# 1088

FCVL	N NUMB	00B8H	A	345#	1090
FEND	N NUMB	00C0H	A	332#	921 930 955 995 1007 1165 1179 1183 1191 1197 1259 1271
FHCNT.	N NUMB	003DH	A	439#	656
FHSS	N NUMB	0038H	A	438#	620 621 624 625 752 753 754 757 758 1605 1609 1612 1641
FLG1	N NUMB	001CH	A	387#	
FLG2	N NUMB	001DH	A	388#	
FLKEY.	D ADDR	00B7H	A	131#	
FLSCL.	D ADDR	00B6H	A	130#	
H1	C ADDR	073FH	A	1615#	1616
H1A.	C ADDR	076EH	A	1638	1640#
H1B.	C ADDR	0734H	A	1607	1609#
H2	C ADDR	01B2H	A	761#	762
H2A.	C ADDR	0103H	A	628#	629
H3	C ADDR	0143H	A	696#	697
H3Z.	C ADDR	0113H	A	644#	645
H4	C ADDR	01ACH	A	755	757#
H4A.	C ADDR	00FDH	A	622	624#
HCFLG.	N NUMB	0011H	A	371#	1120 1213 1225 1244
HELLO.	C ADDR	0717H	A	1496	1589#
HELLO2.	C ADDR	072DH	A	1104	1603#
HELLO_D.	C ADDR	072CH	A	1599#	
HELLO2_D.	C ADDR	0774H	A	1644#	
HT0.	C ADDR	03F9H	A	1120	1123#
HT1.	C ADDR	0406H	A	1123	1129#
HT2.	C ADDR	0408H	A	1128	1130#
HT3.	C ADDR	040AH	A	1122	1131#
HTC0	C ADDR	04BCH	A	1234#	1239
HTC1	C ADDR	04BFH	A	1235#	1238
HTC2	C ADDR	04CEH	A	1243#	
HTC3	C ADDR	04D0H	A	1244#	
HTCMD.	C ADDR	04B4H	A	1121	1230#
HTCT	N NUMB	0040H	A	326#	1211
HTC_D.	C ADDR	04D2H	A	1245#	
HTFLG.	N NUMB	0010H	A	370#	1123 1212 1224
HTG0	C ADDR	0442H	A	1170#	1182
HTG1	C ADDR	0447H	A	1172#	
HTG2	C ADDR	0454H	A	1179	1181#
HTG3	C ADDR	045BH	A	1180	1184#
HTG4	C ADDR	0464H	A	1186	1188#
HTG5	C ADDR	046DH	A	1192#	1192
HTG6	C ADDR	0475H	A	1195#	1195
HTG7	C ADDR	047DH	A	1198#	1198
HTG8	C ADDR	0484H	A	1165	1187 1201#
HTGET.	C ADDR	0435H	A	1118	1163#
HTG_D.	C ADDR	0489H	A	1200	1203#
HTS0	C ADDR	0305H	A	967#	
HTS1	C ADDR	0307H	A	968#	972
HTS2	C ADDR	0309H	A	969#	969
HTS4	C ADDR	0317H	A	973	977#
HTSND.	C ADDR	02ECH	A	778	951#
HTS_D.	C ADDR	031BH	A	979#	
HTT0	C ADDR	049BH	A	1211	1215#
HTT1	C ADDR	04A9H	A	1216	1220 1222#
HTTYP.	C ADDR	048AH	A	1119	1207#
HTT_D.	C ADDR	04B3H	A	1208	1214 1221 1226#
HT_D	C ADDR	040EH	A	1133#	
ID0	B ADDR	0090H.7	A	455#	1507
IDA0CN.	D ADDR	00B9H	A	133#	
IDA0H.	D ADDR	0097H	A	111#	
IDA0L.	D ADDR	0096H	A	110#	
IDAK	N NUMB	003CH	A	295#	
IDBUF.	N NUMB	002DH	A	425#	859 945 985 1223 1250 1505
IDRX	N NUMB	0064H	A	309#	882 943
IDTX	N NUMB	0044H	A	301#	943 945 1223 1635 1636
IE	D ADDR	00A8H	A	124#	
IE0.	B ADDR	0088H.1	A	194#	

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IE1 . . . . . B ADDR 0088H.3 A 192#
IP . . . . . D ADDR 00B8H A 132#
ISR_ON . . . . . C ADDR 0693H A 1508 1513#
IT0 . . . . . B ADDR 0088H.0 A 195#
IT01CF . . . . . D ADDR 00E4H A 164#
IT1 . . . . . B ADDR 0088H.2 A 193#
ITICK. . . . . N NUMB 00E1H A 283# 1482 1483
LD0 . . . . . C ADDR 02C7H A 925# 929
LD1 . . . . . C ADDR 02D6H A 934#
LD_D . . . . . C ADDR 02DAH A 936#
LD_TX. . . . . C ADDR 02B6H A 774 916#
LED. . . . . C ADDR 035FH A 660 662 664 666 667 668 669 670 672 674 676 681 682 683 687 688 689 780
1016# 1240
LED0 . . . . . C ADDR 0364H A 1018# 1022 1023
LED_D. . . . . C ADDR 036DH A 1024#
LNAK . . . . . N NUMB 0039H A 292# 867 888
LNRX . . . . . N NUMB 0061H A 306# 802 815 919 931 954 1047 1497
LNTX . . . . . N NUMB 0041H A 298# 897 920 932 1166 1184 1201 1290 1376 1498 1624 1634
LRXSM. . . . . N NUMB 0002H A 353# 480 483
MAIN . . . . . C ADDR 014DH A 706# 723 724 726 728
MASTER . . . . . B ADDR 00C0H.7 A 226#
MCE0 . . . . . B ADDR 0098H.5 A 199#
MN0 . . . . . C ADDR 0154H A 710 713#
MN1 . . . . . C ADDR 0162H A 713 714 715 716 718#
MN2 . . . . . C ADDR 0167H A 718 720#
MN3 . . . . . C ADDR 016EH A 712 720 723#
MN4 . . . . . C ADDR 0176H A 726#
MN_D . . . . . C ADDR 017BH A 728#
MODF . . . . . B ADDR 00F8H.5 A 274#
MSGT . . . . . N NUMB 0020H A 325# 849 1215
NEW_IO . . . . . C ADDR 0618H A 1444#
NHFLG. . . . . N NUMB 0009H A 360# 973
NSSMD0 . . . . . B ADDR 00F8H.2 A 277#
NSSMD1 . . . . . B ADDR 00F8H.3 A 276#
NXT_TX . . . . . C ADDR 0725H A 1596# 1596
OKFLG. . . . . N NUMB 0007H A 358# 735 1048 1092
OPEN . . . . . B ADDR 0080H.2 A 460# 663 675 866 900 1103 1111
OPENING. . . . . B ADDR 0080H.1 A 459# 661 673
OSCICL . . . . . D ADDR 00B3H A 129#
OSCICN . . . . . D ADDR 00B2H A 128# 1436
OSCLCN . . . . . D ADDR 00E3H A 163#
OSXCXN . . . . . D ADDR 00B1H A 127#
OV . . . . . B ADDR 00D0H.2 A 250#
P . . . . . B ADDR 00D0H.0 A 252#
P0 . . . . . D ADDR 0080H A 91# 451 452 453 458 459 460 461
P0MDIN . . . . . D ADDR 00F1H A 173#
P0MDOUT. . . . . D ADDR 00A4H A 121# 1439 1445 1451
P0SKIP . . . . . D ADDR 00D4H A 153# 1447 1453
P1 . . . . . D ADDR 0090H A 104# 443 444 447 448 455
P1MDIN . . . . . D ADDR 00F2H A 174#
P1MDOUT. . . . . D ADDR 00A5H A 122# 1440 1446 1452
P1SKIP . . . . . D ADDR 00D5H A 154#
P2 . . . . . D ADDR 00A0H A 117#
P2MDOUT. . . . . D ADDR 00A6H A 123#
PCA0CN . . . . . D ADDR 00D8H A 155#
PCA0CPH0 . . . . . D ADDR 00FCH A 180#
PCA0CPH1 . . . . . D ADDR 00EAH A 168#
PCA0CPH2 . . . . . D ADDR 00ECH A 170#
PCA0CPL0 . . . . . D ADDR 00FBH A 179#
PCA0CPL1 . . . . . D ADDR 00E9H A 167#
PCA0CPL2 . . . . . D ADDR 00EBH A 169#
PCA0CPM0 . . . . . D ADDR 00DAH A 157#
PCA0CPM1 . . . . . D ADDR 00DBH A 158#
PCA0CPM2 . . . . . D ADDR 00DCH A 159#
PCA0H. . . . . D ADDR 00FAH A 178#
PCA0L. . . . . D ADDR 00F9H A 177#

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PCA0MD . . . . . D ADDR 00D9H A 156# 1435
PCON . . . . . D ADDR 0087H A 95#
PCRCV. . . . . B ADDR 0080H.2 A 451# 916 935 951 978 984 1010 1102 1106 1116 1132 1137 1146 1151 1158
1249 1275
PIFLG. . . . . N NUMB 0018H A 381# 716 741 772 907 910
PI_D . . . . . C ADDR 0423H A 1147#
PMFLG. . . . . N NUMB 0019H A 382# 726 946 1144
PS0. . . . . B ADDR 00B8H.4 A 219#
PSCTL. . . . . D ADDR 008FH A 103#
PSP10. . . . . B ADDR 00B8H.6 A 217#
PSW. . . . . D ADDR 00D0H A 151# 473 613
PT0. . . . . B ADDR 00B8H.1 A 222# 1484
PT1. . . . . B ADDR 00B8H.3 A 220#
PT2. . . . . B ADDR 00B8H.5 A 218#
PX0. . . . . B ADDR 00B8H.0 A 223#
PX1. . . . . B ADDR 00B8H.2 A 221#
RAFLG. . . . . N NUMB 000BH A 363# 740 861 989 1363
RA_D . . . . . C ADDR 03E9H A 1100 1112#
RB80 . . . . . B ADDR 0098H.2 A 202#
RCFLG. . . . . N NUMB 000DH A 365# 769 853 911 1051
REFOCN . . . . . D ADDR 00D1H A 152#
RENO . . . . . B ADDR 0098H.4 A 200#
RESET. . . . . C ADDR 0000H A 467#
RFIC . . . . . C ADDR 069EH A 679 1521#
RFRCV. . . . . B ADDR 0080H.2 A 452# 899 934 977 1009 1054 1091 1231 1241
RHFLG. . . . . N NUMB 001BH A 385# 842 1366
RI0. . . . . B ADDR 0098H.0 A 204# 713 784 1164 1175 1274 1370 1517
RMYC. . . . . N NUMB 0019H A 408# 806 811 821 917 918 924 929 952 953 958 960 962 964 966 972 1045
RMFCC. . . . . N NUMB 001CH A 411# 807 812 814 821 825 1046
RMFCS. . . . . N NUMB 001AH A 409# 822 1062 1064
RMFLG. . . . . N NUMB 000CH A 364# 777 850 1050
RMSBC. . . . . N NUMB 001BH A 410# 513 530 533
RS0. . . . . B ADDR 00D0H.3 A 249#
RS1. . . . . B ADDR 00D0H.4 A 248#
RSFLG. . . . . N NUMB 0017H A 379# 568 710 1109
RSFLG2 . . . . . N NUMB 001FH A 390#
RSTSRC . . . . . D ADDR 00EFH A 171#
RSVT . . . . . N NUMB 0000H A 323#
RTFLG. . . . . N NUMB 0016H A 378# 566 601 724 736 779 1509
RTFLG1 . . . . . N NUMB 001EH A 389#
RTID . . . . . N NUMB 0030H A 429# 1635 1640
RTST_SU. . . . . C ADDR 068AH A 1507#
RTHH . . . . . N NUMB 0031H A 430# 567 569 1510
RTTM . . . . . N NUMB 0002H A 337# 569 1510
RT_D . . . . . C ADDR 0434H A 1159#
RX0. . . . . C ADDR 0198H A 741 743#
RX1. . . . . C ADDR 019CH A 740 745#
RX2. . . . . C ADDR 01C1H A 769 772#
RX3. . . . . C ADDR 01CDH A 772 773 777#
RX4. . . . . C ADDR 01D2H A 735 736 738 744 771 776 777 779#
RX5. . . . . C ADDR 01D7H A 779 781#
RXBB . . . . . N NUMB 0018H A 407# 531 791 797 1044
RXBH . . . . . N NUMB 0017H A 406# 506 508 794 799 800 801 803 1042
RXBIT. . . . . N NUMB 0003H A 354# 491 503 527
RXBL . . . . . N NUMB 0016H A 405# 500 505 510 512 524 529 531 532 1043
RXC0 . . . . . C ADDR 02AEH A 906 909#
RXC1 . . . . . C ADDR 02B3H A 908 909 911#
RXCMD. . . . . C ADDR 02A5H A 770 905#
RXCT . . . . . N NUMB 0080H A 327# 852 1219
RXC_D. . . . . C ADDR 02B5H A 912#
RXF0 . . . . . C ADDR 021DH A 822# 825
RXFCS. . . . . C ADDR 021AH A 734 821#
RXF_D. . . . . C ADDR 0227H A 827#
RXI . . . . . B ADDR 0080H.3 A 453# 518 816 1055 1232 1242
RXM2 . . . . . C ADDR 01EBH A 795# 795
RXM3 . . . . . C ADDR 020BH A 805 811#

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RXM4 . . . . . C ADDR 0211H A 802 810 813#
RXMB . . . . . N NUMB 0060H A 305#
RXMSG. . . . . C ADDR 01E0H A 732 789# 789 814
RXM_D. . . . . C ADDR 0219H A 817#
RXOVRN . . . . . B ADDR 00F8H.4 A 275#
RXPIN. . . . . B ADDR 0090H.4 A 447# 481
RXRST. . . . . C ADDR 037DH A 781 1041#
RXR_D. . . . . C ADDR 039AH A 1056#
RXSFLG . . . . . N NUMB 0005H A 356# 515 534 609 789 790 795 796
RXSMP. . . . . N NUMB 0001H A 352# 479 482 490
RXT0 . . . . . C ADDR 024CH A 849 852#
RXT1 . . . . . C ADDR 0253H A 852 855#
RXT0 . . . . . C ADDR 0228H A 737 831#
RXT0_D . . . . . C ADDR 0240H A 837 841 843#
RXTYP. . . . . C ADDR 0241H A 739 847#
RXT_D. . . . . C ADDR 0260H A 851 854 855 858 862#
RX_D . . . . . C ADDR 01DFH A 785#
RX_SMBL. . . . . C ADDR 078BH A 514 1672#
SOMODE . . . . . B ADDR 0098H.7 A 198#
SBUF0. . . . . D ADDR 0099H A 113# 968 995 998 1001 1004 1007 1163 1174 1191 1194 1197 1259 1262 1265
1268 1271 1595
SCON0. . . . . D ADDR 0098H A 112# 1491
SETUP. . . . . C ADDR 0601H A 654 1434#
SETUP_D. . . . . C ADDR 069DH A 1518#
SET_CK . . . . . C ADDR 0603H A 1435#
SET_IO . . . . . C ADDR 060CH A 1438#
SET_SPIO . . . . . C ADDR 0636H A 1458#
SI . . . . . B ADDR 00C0H.0 A 233#
SIFLG. . . . . N NUMB 000EH A 367# 715 933 1129 1188 1243 1368 1495
SIHLD. . . . . N NUMB 0008H A 359# 516 714 1053 1494
SMBOCF . . . . . D ADDR 00C1H A 140#
SMBOCN . . . . . D ADDR 00C0H A 139#
SMBODAT. . . . . D ADDR 00C2H A 141#
SND_H. . . . . C ADDR 071FH A 1592# 1598
SND_H2 . . . . . C ADDR 0758H A 1628# 1633
SNFLG. . . . . N NUMB 000AH A 361# 590 720 1364
SOPFLG . . . . . N NUMB 0004H A 355# 496 517 535 602 723 1052 1513
SOPH . . . . . N NUMB 00E2H A 335# 509
SOPL . . . . . N NUMB 00E2H A 334# 511
SP . . . . . D ADDR 0081H A 92#
SPIOCFG. . . . . D ADDR 00A1H A 118# 1460
SPIOCKR. . . . . D ADDR 00A2H A 119# 1462
SPIOCN . . . . . D ADDR 00F8H A 176# 1461
SPIODAT. . . . . D ADDR 00A3H A 120#
SPIEN. . . . . B ADDR 00F8H.0 A 279#
SPIF . . . . . B ADDR 00F8H.7 A 272#
SPIOCFG. . . . . N NUMB 00A1H A 315#
SPIOCKR. . . . . N NUMB 00A2H A 316#
SPIOCN . . . . . N NUMB 00F8H A 314# 1578
SPIODAT. . . . . N NUMB 00A3H A 317# 617 630 639 646 691 698 750 763 1522 1524 1526 1528 1530 1532 1534
1536 1538 1540 1542 1544 1546 1548 1550 1552 1554 1556 1564 1566 1571 1573
1610 1617
618 640 647 692 699 751 764 1523 1525 1527 1529 1531 1533 1535 1537 1539
1541 1543 1545 1547 1549 1551 1553 1555 1557 1565 1567 1572 1574 1577#
1580 1611 1618
SPIO_WAIT. . . . . C ADDR 070FH A
STA. . . . . B ADDR 00C0H.5 A 228#
START. . . . . C ADDR 00FFH A 467 654#
STO. . . . . B ADDR 00C0H.4 A 229#
STX. . . . . N NUMB 0002H A 329#
T2SPLIT. . . . . B ADDR 00C8H.3 A 240#
T2XCLK . . . . . B ADDR 00C8H.0 A 242#
TABLE. . . . . C ADDR 07D3H A 1589 1748#
TACK . . . . . N NUMB 0006H A 330#
TB80 . . . . . B ADDR 0098H.3 A 201#
TBL_2. . . . . C ADDR 07E1H A 1625 1763#
TCON . . . . . D ADDR 0088H A 96#

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TEMPB.	N NUMB	002FH	A	427# 889 898
TF0.	B ADDR	0088H.5	A	190# 1481
TF1.	B ADDR	0088H.7	A	188# 1488
TF2CEN.	B ADDR	00C8H.4	A	239#
TF2H.	B ADDR	00C8H.7	A	236#
TF2L.	B ADDR	00C8H.6	A	237#
TF2LEN.	B ADDR	00C8H.5	A	238#
TFAK.	N NUMB	003BH	A	294#
TFBUF.	N NUMB	002EH	A	426# 831 856 944 992 1222 1256 1504
TFRX.	N NUMB	0063H	A	308# 834 858 876 940
TFTX.	N NUMB	0043H	A	300# 942 944 1222
TH0.	D ADDR	008CH	A	100# 1482
TH1.	D ADDR	008DH	A	101# 1489
THFLG.	N NUMB	001AH	A	384# 738 838 1049
TI0.	B ADDR	0098H.1	A	203# 783 967 969 970 976 994 996 997 999 1000 1002 1003 1005 1006 1008 1190 1192 1193 1195 1196 1198 1199 1258 1260 1261 1263 1264 1266 1267 1269 1270 1272 1273 1369 1516 1594 1596
TIC0.	C ADDR	007FH	A	475 539#
TIC1.	C ADDR	008CH	A	539 541 548#
TIC2.	C ADDR	009BH	A	548 551 557#
TIC2_C.	C ADDR	00A1H	A	562#
TIC3.	C ADDR	00AFH	A	565 566 567 573#
TICK.	C ADDR	000BH	A	473#
TICK_D.	C ADDR	00CAH	A	535 559 573 574 588 594#
TICK_D1.	C ADDR	00E8H	A	594 595 601 604 609#
TICK_D2.	C ADDR	00E0H	A	596 605#
TICK_D3.	C ADDR	00EBH	A	609 611#
TICK_SU.	C ADDR	064CH	A	1479#
TL0.	D ADDR	008AH	A	98# 1483
TL1.	D ADDR	008BH	A	99# 580 1490
TMBIC.	N NUMB	0024H	A	416# 1309 1317 1332 1333 1348 1349
TMBYC.	N NUMB	0026H	A	418# 889 890 898 918 1169 1178 1181 1185 1202 1207 1280 1281 1282 1320 1387 1627 1628 1631
TMBYT.	N NUMB	0025H	A	417# 893 1308 1310 1312 1323 1327 1378
TMFCC.	N NUMB	001EH	A	414# 549 550 553 1170 1282 1283 1284 1288 1379
TMFCS.	N NUMB	0029H	A	421# 869 873 879 884 1285 1396 1398
TMFLG.	N NUMB	0013H	A	374# 575 589 718 1156
TMOD.	D ADDR	0089H	A	97# 1479
TMR2CN.	D ADDR	00C8H	A	146#
TMR2H.	D ADDR	00CDH	A	150#
TMR2L.	D ADDR	00CCH	A	149#
TMR2RLH.	D ADDR	00CBH	A	148#
TMR2RL.	D ADDR	00CAH	A	147#
TMR3CN.	D ADDR	0091H	A	105#
TMR3H.	D ADDR	0095H	A	109#
TMR3L.	D ADDR	0094H	A	108#
TMR3RLH.	D ADDR	0093H	A	107#
TMR3RL.	D ADDR	0092H	A	106#
TNAK.	N NUMB	0015H	A	331#
TOFLG.	N NUMB	000FH	A	368# 548 552 1171 1189
TPAK.	N NUMB	003AH	A	293#
TFRX.	N NUMB	0062H	A	307# 839 847
TFTX.	N NUMB	0042H	A	299# 1209 1217
TR0.	B ADDR	0088H.4	A	191# 1480 1486
TR1.	B ADDR	0088H.6	A	189# 1487 1493
TR2.	B ADDR	00C8H.2	A	241#
TSFLG.	N NUMB	0014H	A	375# 539 565 1304 1355
TSTRT.	C ADDR	0775H	A	1300 1648#
TXBIT.	N NUMB	0015H	A	376# 542 1315 1346
TXBMT.	B ADDR	00F8H.1	A	278#
TXCNT.	N NUMB	002CH	A	424# 587 988 1127 1142 1154 1388
TXF0.	C ADDR	051CH	A	1285# 1288
TXFCS.	C ADDR	0511H	A	1105 1124 1139 1280#
TXFLG.	N NUMB	0012H	A	373# 573 773 1100 1126 1141 1365 1383
TXF_D.	C ADDR	0528H	A	1291#
TXM0.	C ADDR	055DH	A	1319#

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TXM1 . . . . . C ADDR 0563H A 1321# 1352
TXM2 . . . . . C ADDR 0577H A 1333# 1351
TXM3 . . . . . C ADDR 0585H A 1336 1341#
TXM4 . . . . . C ADDR 058AH A 1340 1344# 1345
TXM5 . . . . . C ADDR 059BH A 1350 1352#
TXM6 . . . . . C ADDR 059EH A 1353# 1354
TXMB . . . . . N NUMB 0040H A 297#
TXMODE . . . . . B ADDR 00C0H.6 A 227#
TXMRS. . . . . C ADDR 05A9H A 722 743 1363#
TXMSG. . . . . C ADDR 0529H A 891 1107 1125 1140 1153 1295#
TXM_D. . . . . C ADDR 05A8H A 1359#
TXP0 . . . . . C ADDR 052EH A 1299# 1299
TXPIN. . . . . B ADDR 0090H.3 A 448# 543 1356 1472
TXRST. . . . . C ADDR 05BAH A 1108 1130 1143 1155 1367 1376#
TXR_D. . . . . C ADDR 05D0H A 1383 1390#
TXS0 . . . . . C ADDR 053FH A 1305# 1318
TXS1 . . . . . C ADDR 0549H A 1310# 1317
TXS2 . . . . . C ADDR 054EH A 1313# 1314
TXSH . . . . . N NUMB 0028H A 420# 896 1331 1337 1339 1382
TXSI . . . . . N NUMB 001DH A 413# 1301 1305 1306
TXSL . . . . . N NUMB 0027H A 419# 895 1326 1341 1343 1381
TXSMC. . . . . N NUMB 001FH A 415# 540 544 894 1303 1313 1316 1344 1347 1353 1380
TXS_D. . . . . C ADDR 05B9H A 1371#
TXTH . . . . . N NUMB 002BH A 423# 574 583 1389
TXTL . . . . . N NUMB 002AH A 422# 557 558
TX_OFF. . . . . C ADDR 0704H A 685 1357 1570#
TX_ON. . . . . C ADDR 06F9H A 1295 1563#
TX_SMBL. . . . . C ADDR 077BH A 1319 1655#
UART_SU. . . . . C ADDR 065FH A 1487#
VDMOCN. . . . . D ADDR 00FFH A 181#
WAIT . . . . . C ADDR 036EH A 648 700 1028# 1619 1620 1621
WAIT0. . . . . C ADDR 0373H A 1030# 1034 1035
WAIT_D. . . . . C ADDR 037CH A 1036#
WCOL . . . . . B ADDR 00F8H.6 A 273#
XBR0 . . . . . D ADDR 00E1H A 161# 1441 1448 1454
XBR1 . . . . . D ADDR 00E2H A 162# 1442 1449 1455
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REGISTER BANK(S) USED: 0

ASSEMBLY COMPLETE. 0 WARNING(S), 0 ERROR(S)

Bob Nelson
RF Monolithics
2/7/2007